A 400MT/s 6.4GB/s Multiprocessor Bus Interface

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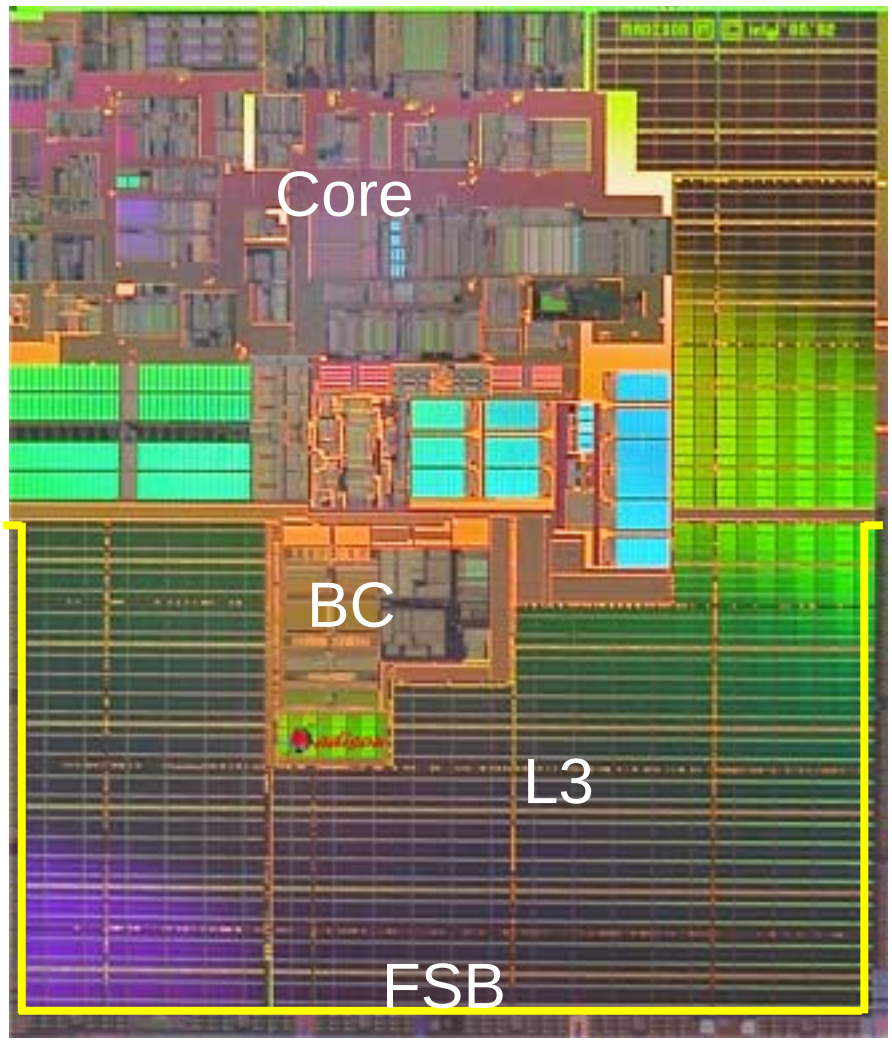
Agenda

- Itanium® 2 Processor Overview
- Package Design
- I/O buffer Design
- I/O Loopback Test
- Interpolator
- Modeling and Validation

Intel Itanium® 2 Processor (Madison)

- EPIC architecture
- 0.13u process technology
- 6-layer copper
- 1.5GHz, 1.3V core
- 6MB on-die L3 cache
- Enterprise-class RAS, DFT & DFM features

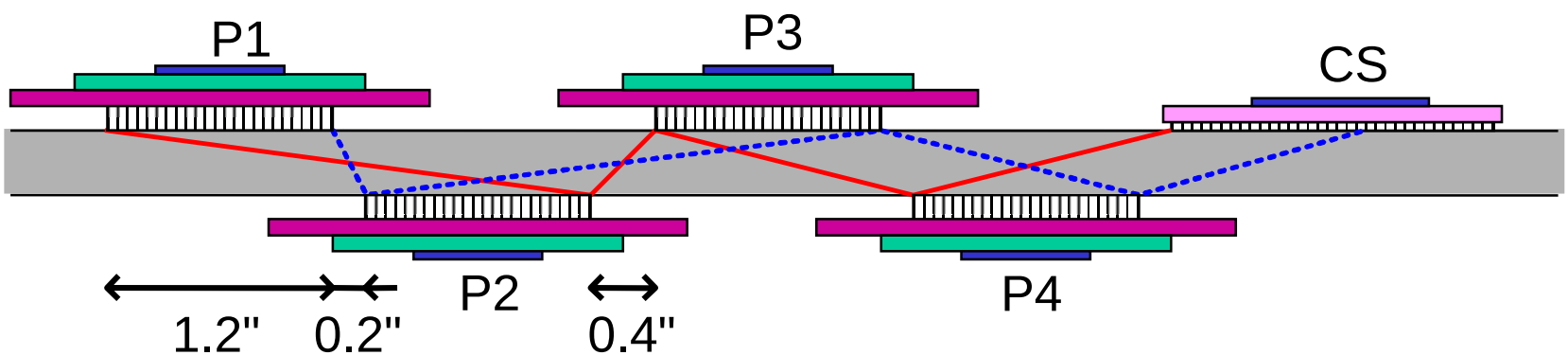


Front-Side Bus

Interface Support	Glueless 4-way Multi-Processor
Output Voltage	GTL+ compatible, 400mV-1.2V
Voltage Reference	0.75V on-die generated vref
Data Bus Width	16 bytes
Data Bus Speed	400MT/s source synchronous
Data Strobing	1 differential strobe per 2B of data
Peak BW	6.4GB/s
Addr, Control Speed	200MHz common clock

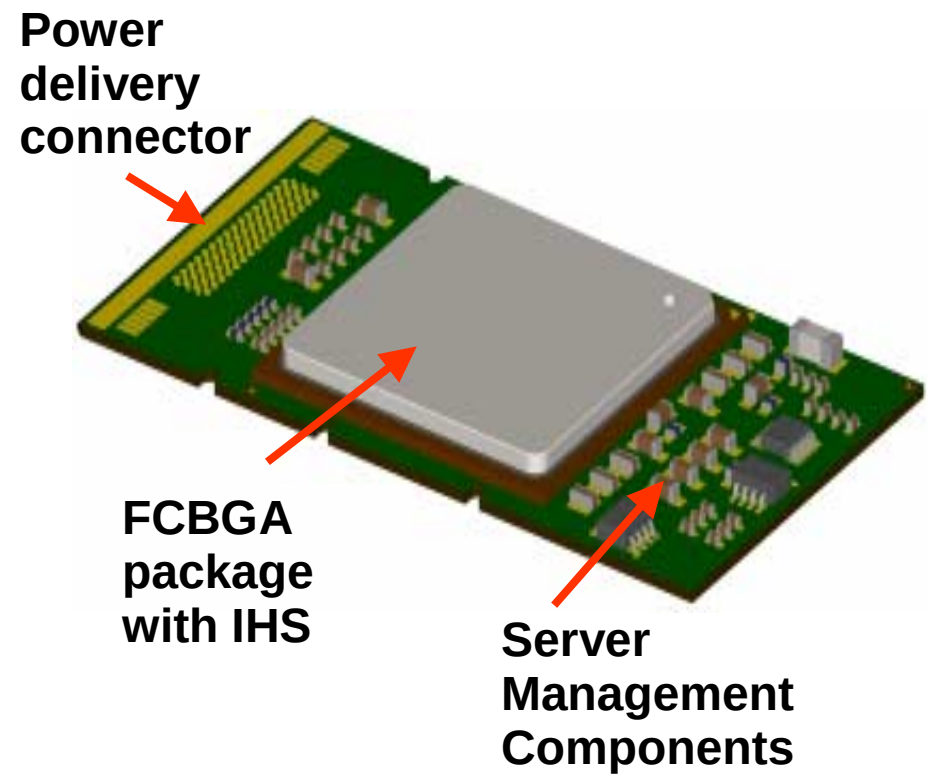
System Topology

- Double-sided placement
- Total net length is 6.4 to 6.8 inches
- Staggered placement of through-hole vias
- Data and strobe are matched for length, layer & number of vias



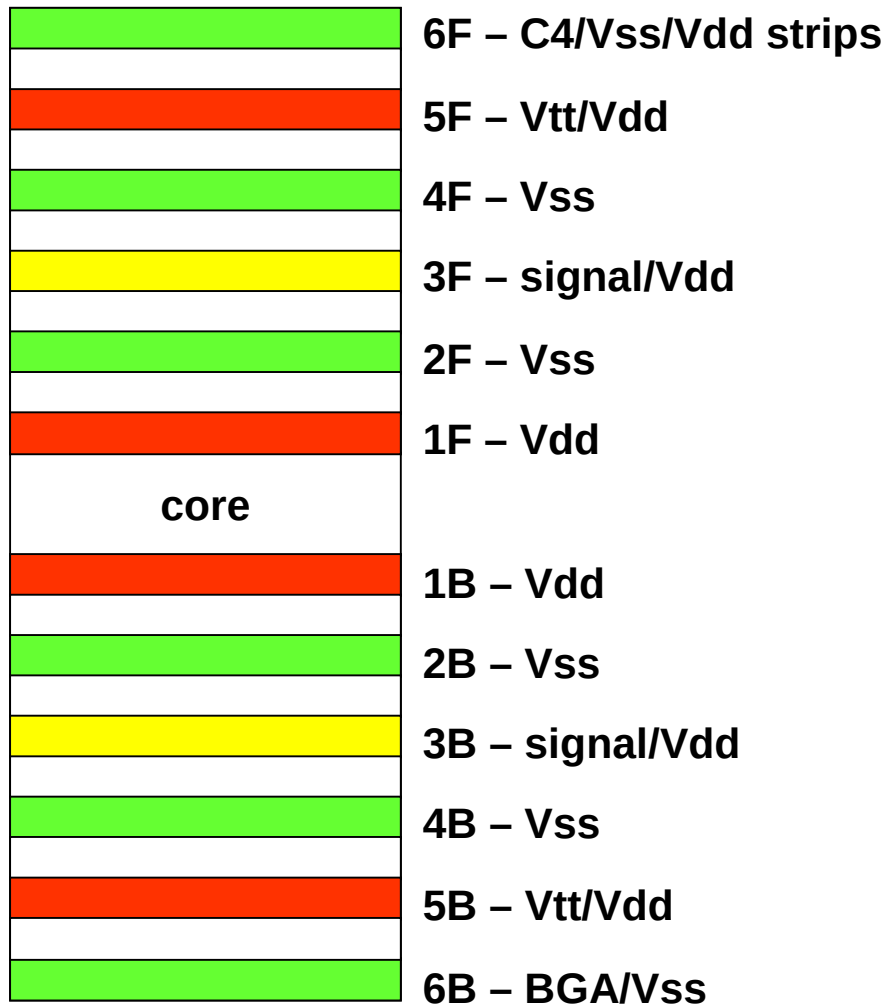
Package Design

- Multi-level packaging
  - Low inductance power delivery
  - Space transformer
- CPU is on organic substrate mounted on interposer
- Ground-referenced striplines
- Maximum trace length
  - 12mm max length for SS signal
  - 18mm for CC signals
- Zo = 45ohm +/- 12%



Processor Package

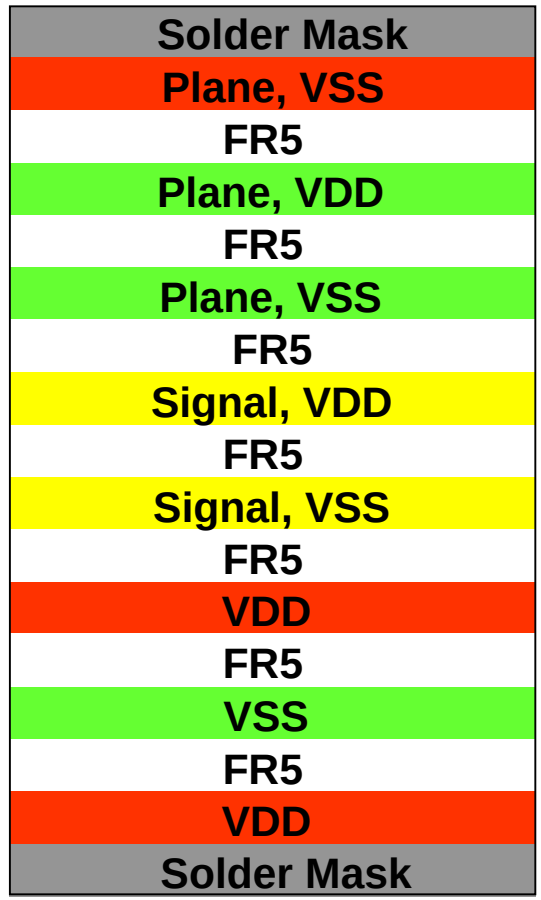
- 12-layer organic substrate
- 42.5 x 42.5 mm
- 2 signal layers
  - Ground referenced
  - Space transformation from C4 bumps to BGA balls



Package stack-up

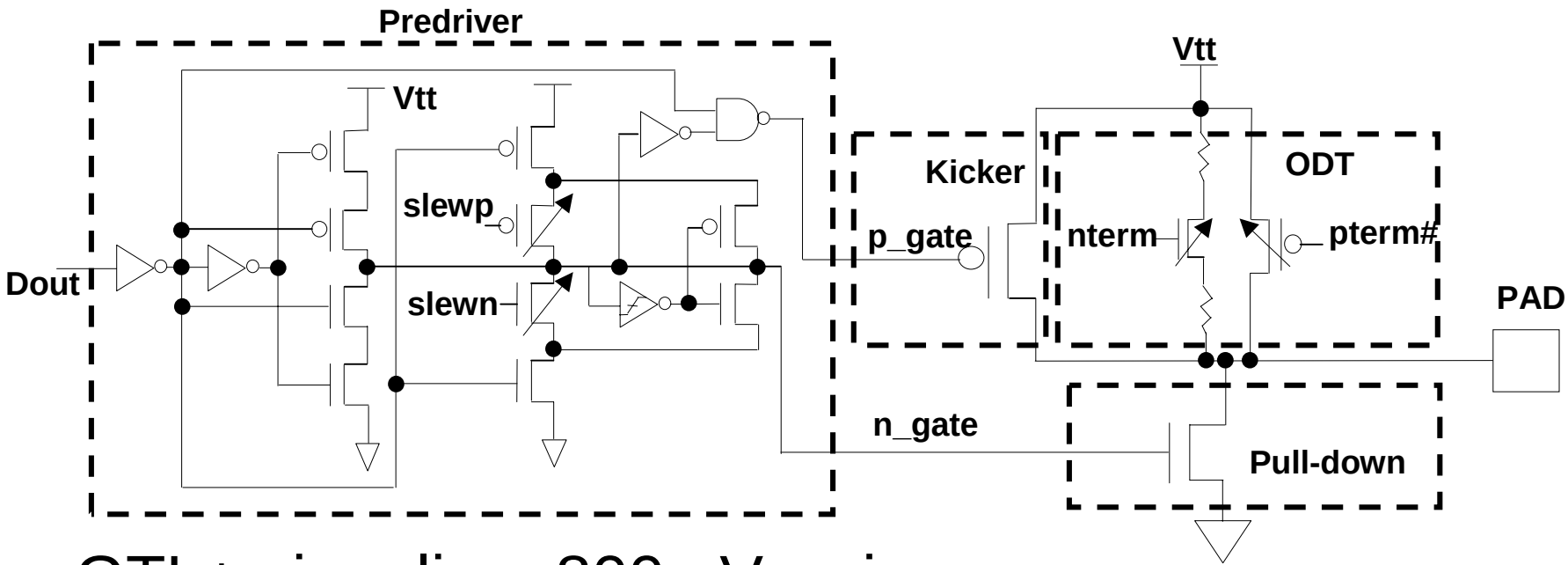
Package Interposer

- 8-layer interposer
  - Core power delivery through power pod
  - Other power & signals through pins
- 50 mils pitch
  - 311 signals
  - 60 I/O power pins
  - 233 ground pins
  - 5:1:4 signal:vtt:vss



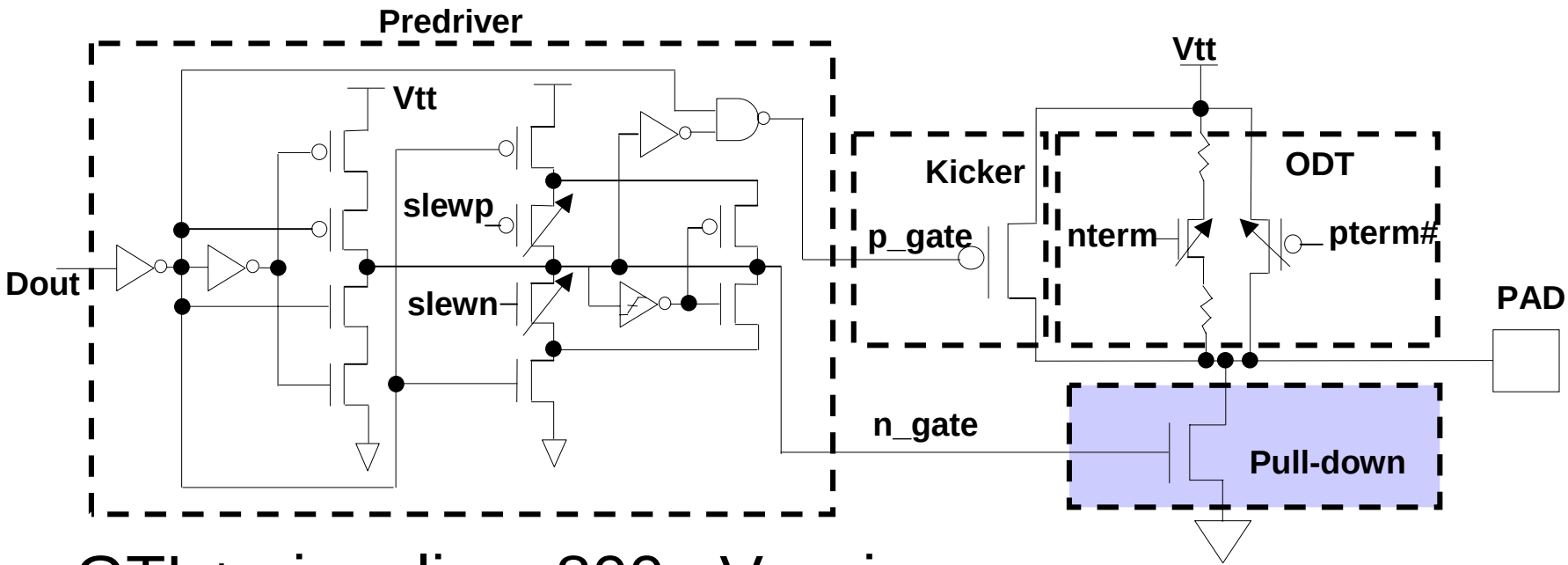
Interposer stack-up

Output Buffer



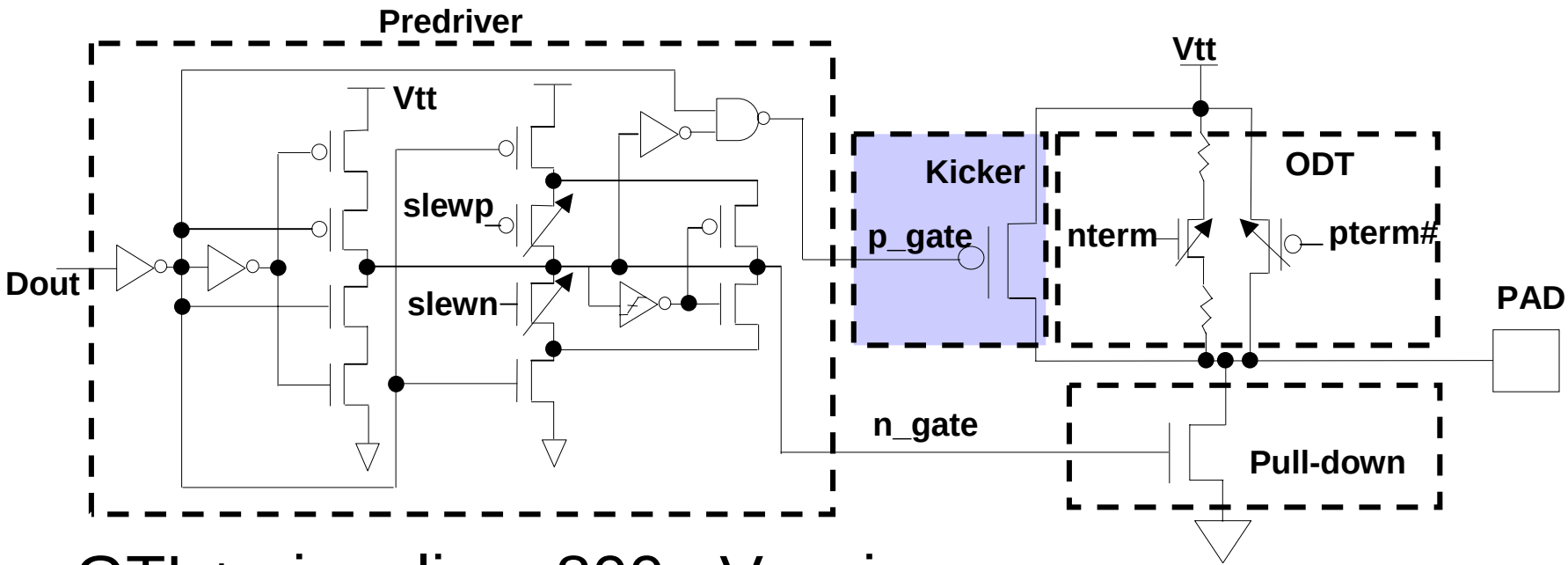
- GTL+ signaling, 800mV swing

Output Buffer



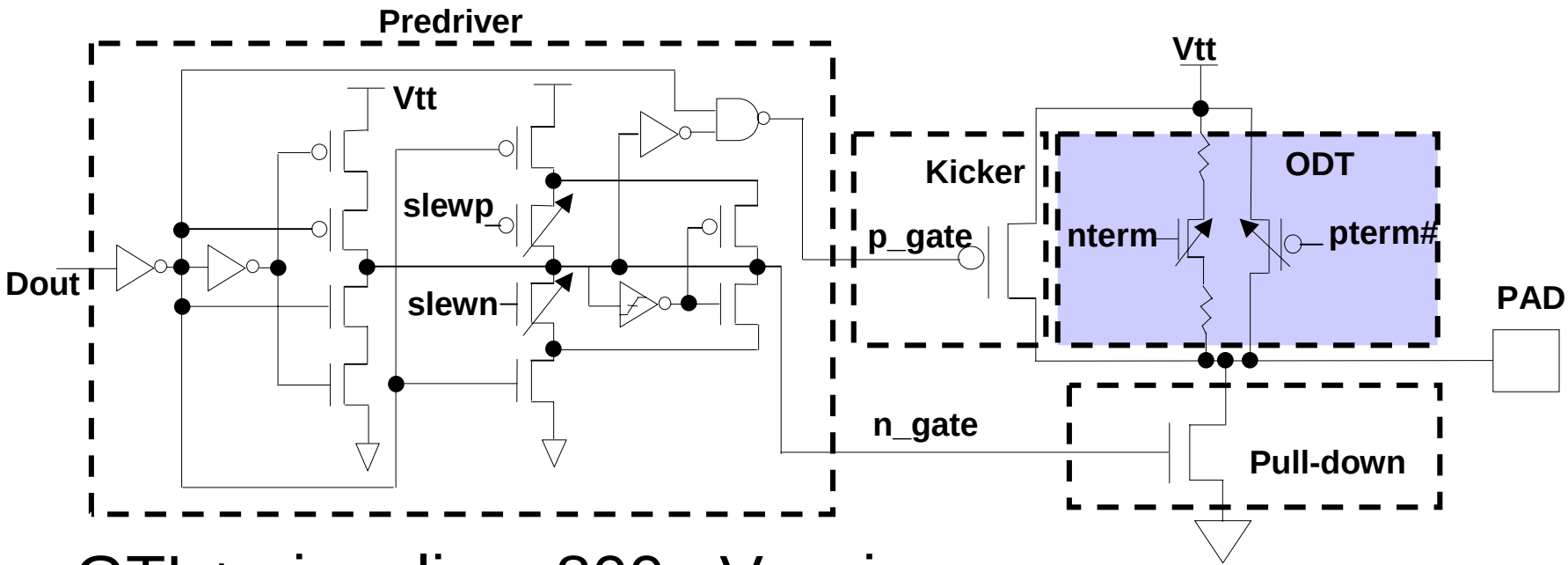
- GTL+ signaling, 800mV swing
- 5-8ohm NMOS pull-down

Output Buffer



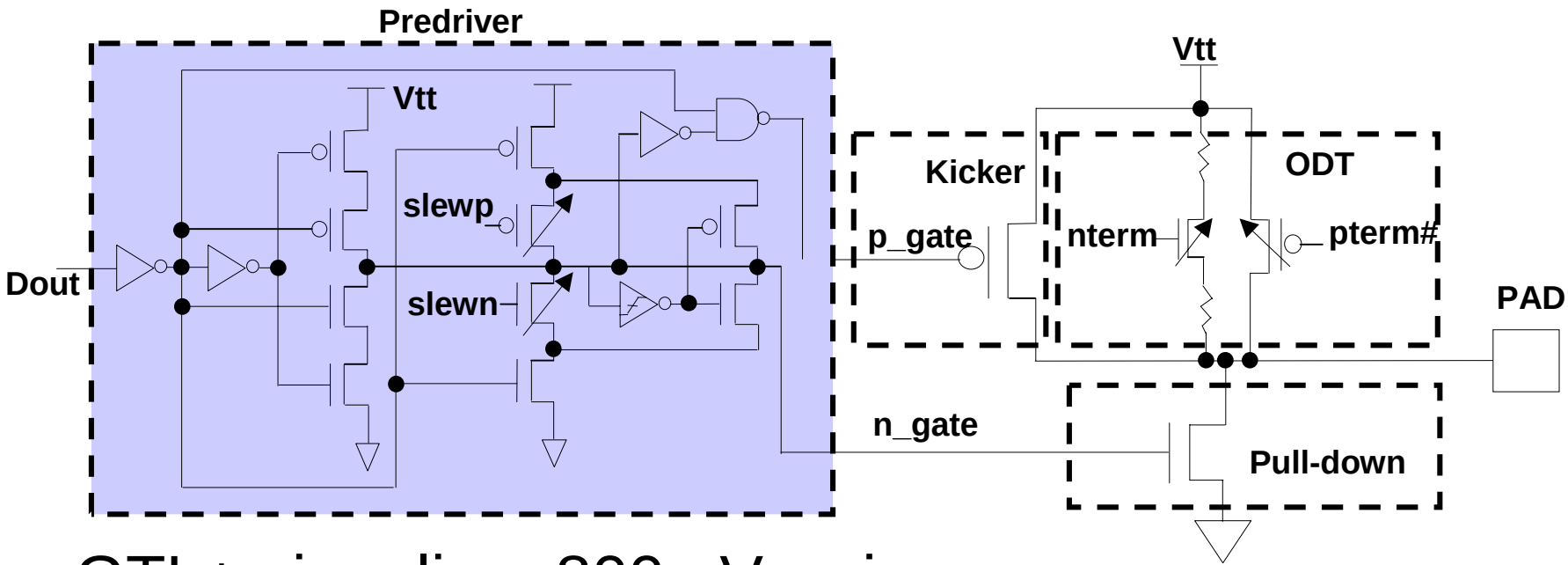
- GTL+ signaling, 800mV swing
- 5-8ohm NMOS pull-down
- 40-60ohm PMOS kicker pullup

Output Buffer



- GTL+ signaling, 800mV swing
- 5-8ohm NMOS pull-down
- 40-60ohm PMOS kicker pullup
- 45 ohm on-die terminator (ODT)

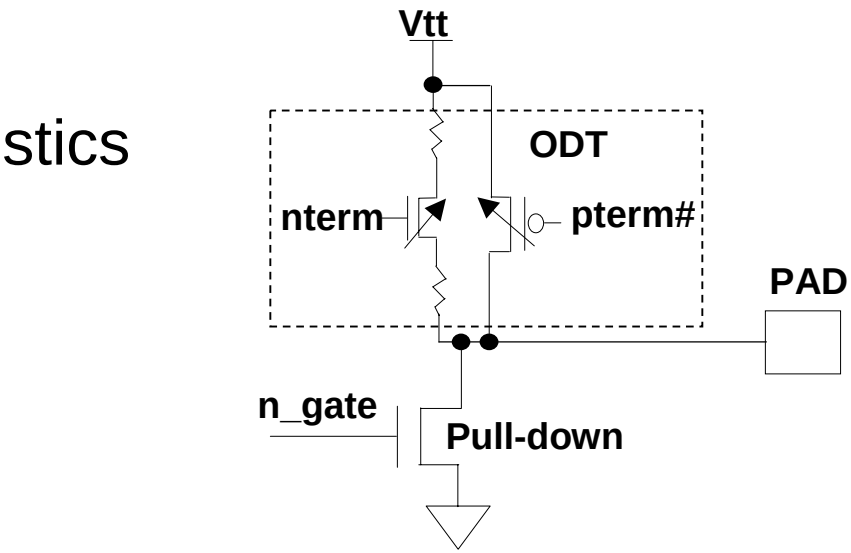
Output Buffer

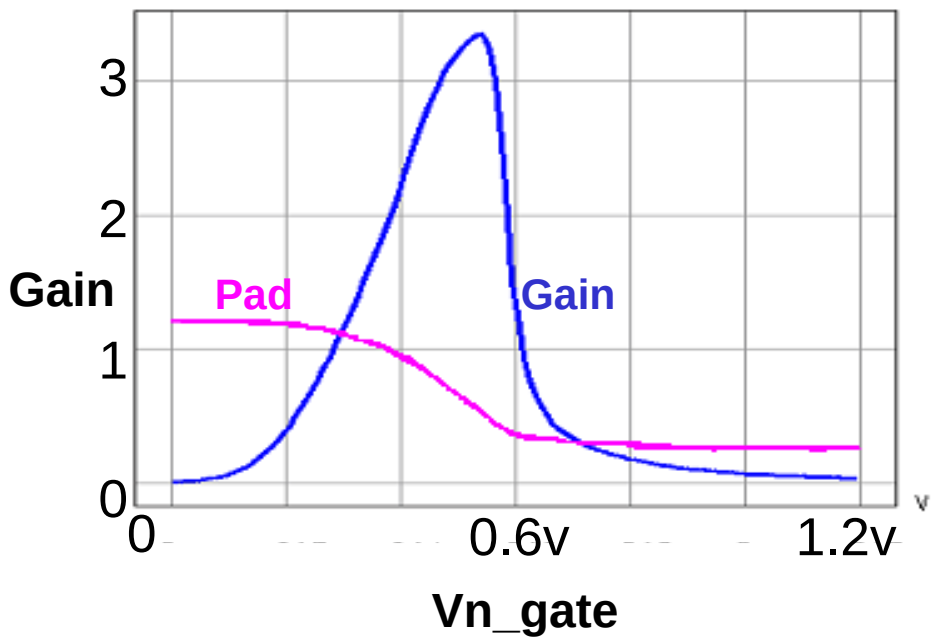


- GTL+ signaling, 800mV swing
- 5-8ohm NMOS pull-down
- 40-60ohm PMOS kicker pullup
- 45 ohm on-die terminator (ODT)
- 1V/ns slew-rate control

Output Buffer Gain Curve

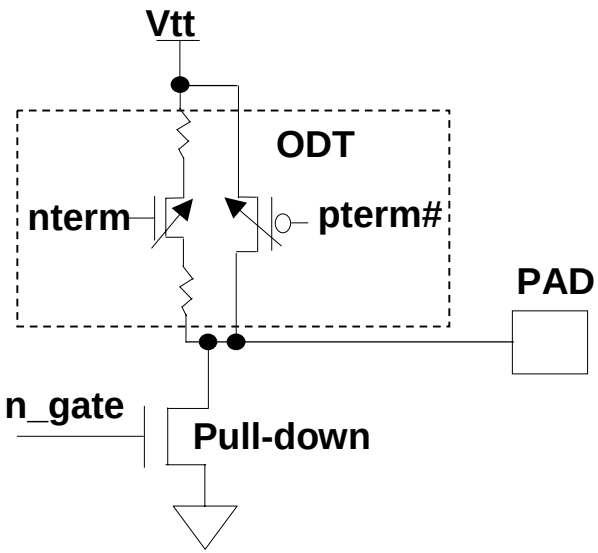
- Output buffer gain characteristics is non-linear

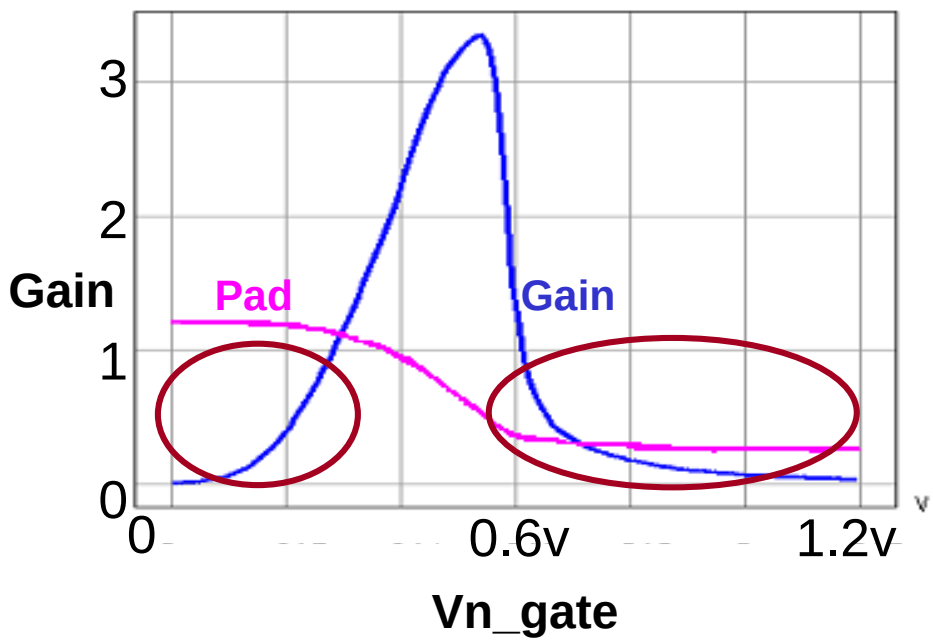




Output Buffer Gain Curve

- Output buffer gain characteristics is non-linear
- Gain is low in
  - cut-off
  - linear region





Output Buffer Gain Curve

- Output buffer gain characteristics is non-linear
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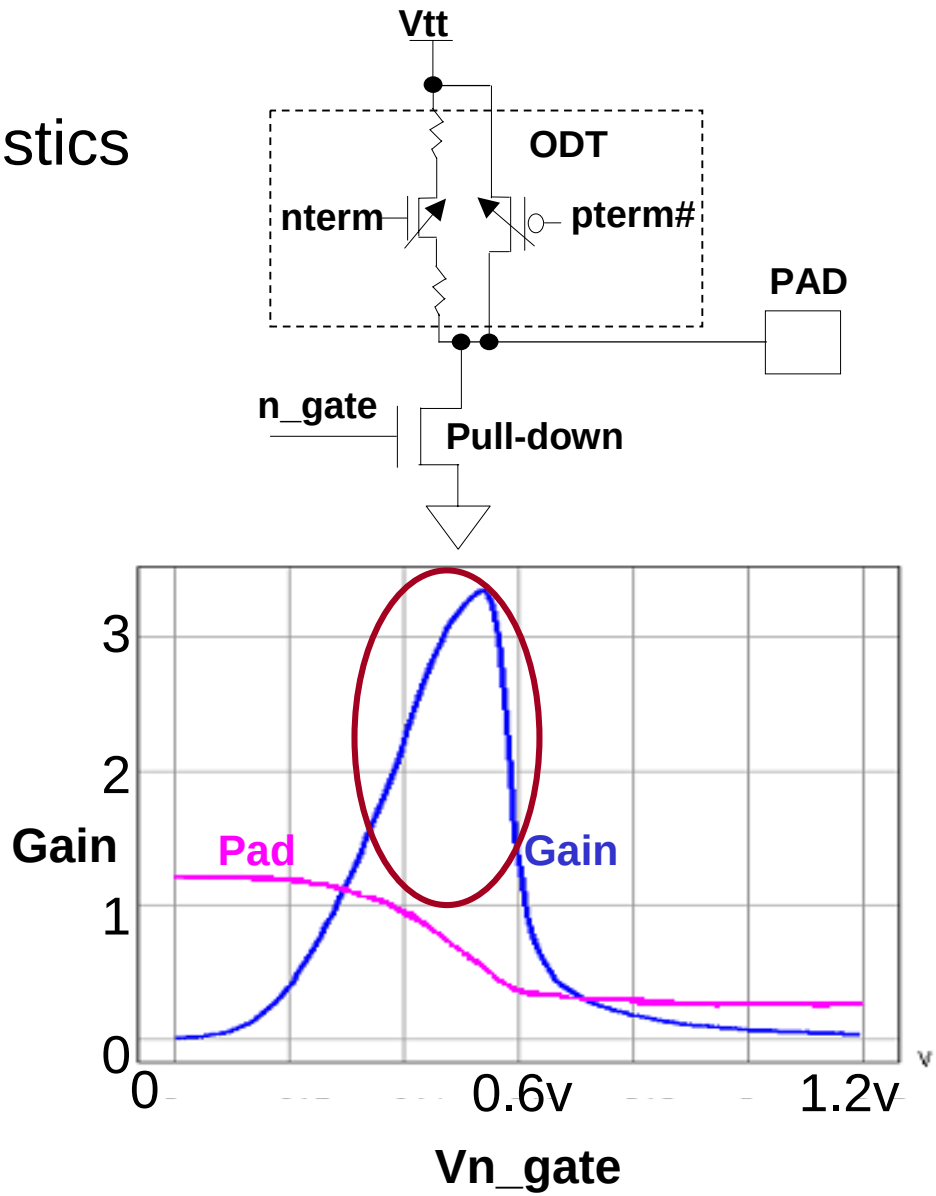
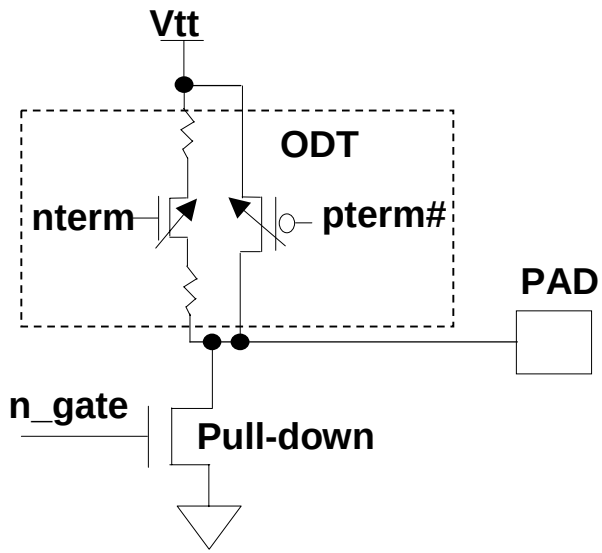
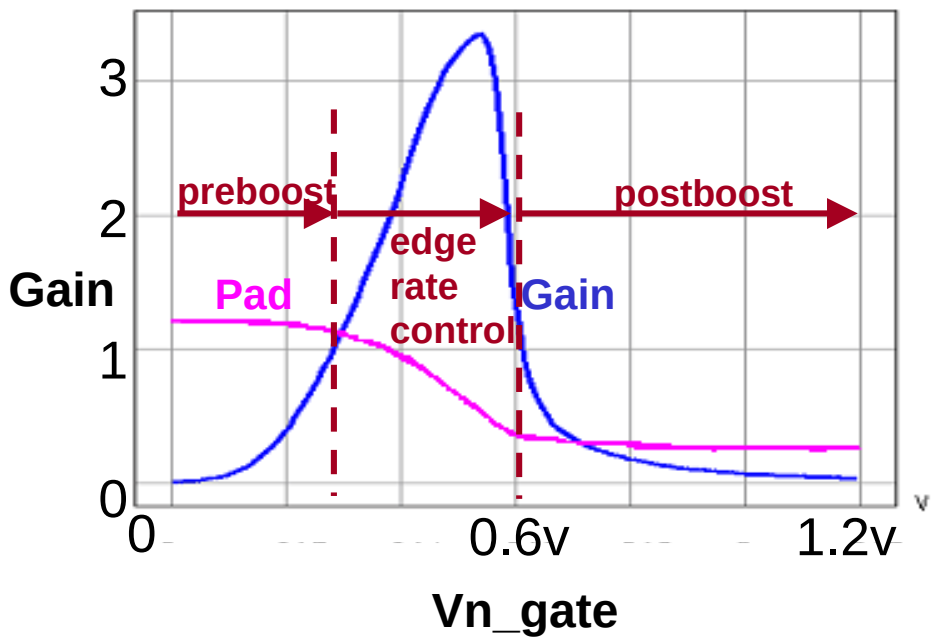
- Gain is high in saturation



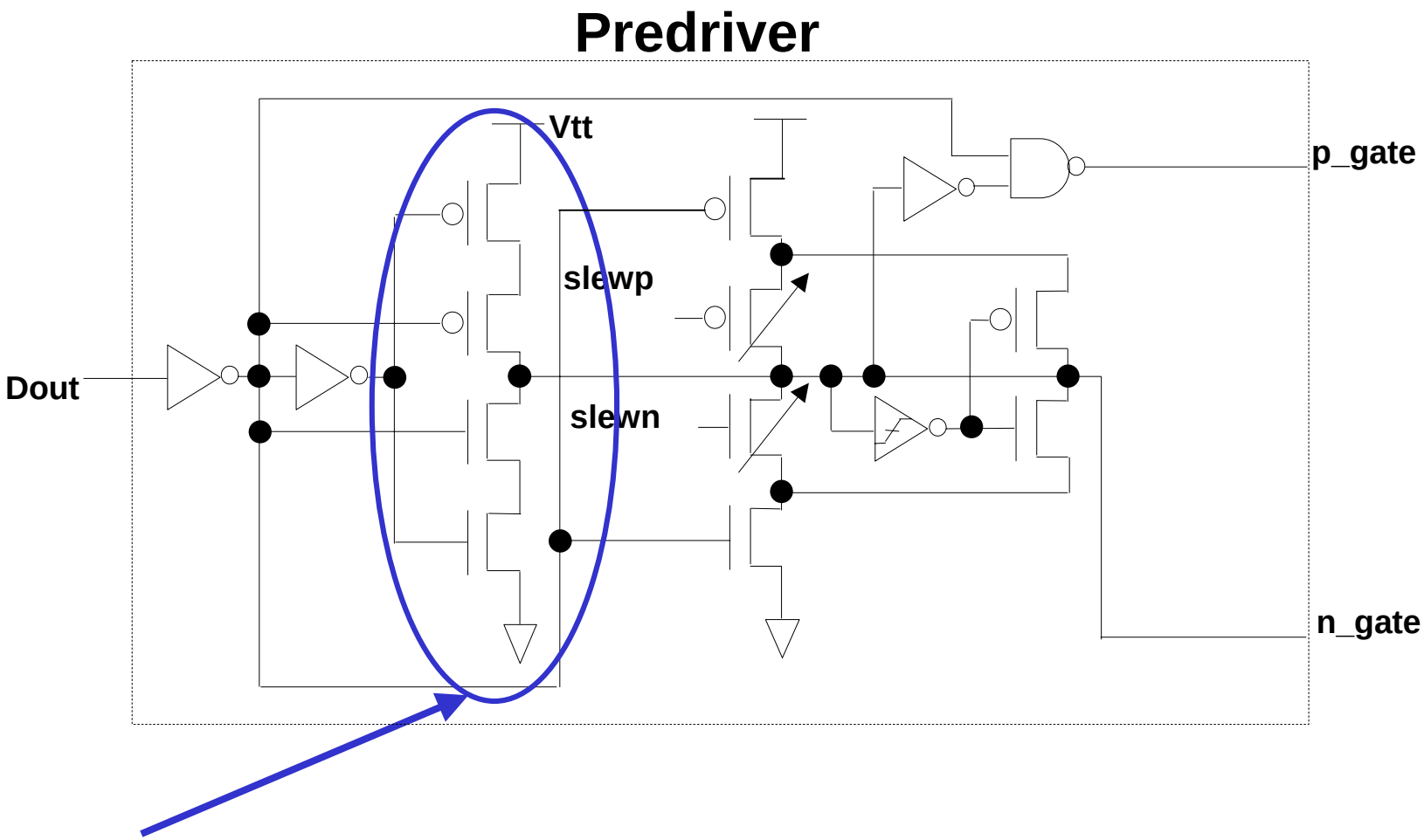
Output Buffer Gain Curve

- Output buffer gain characteristics is non-linear
- Gain is low in
  - cut-off
  - linear region
- Gain is high in saturation
- n_gate transitions rapidly
  - 0v to 0.3v (preboost)
  - 0.6v to 1.2v (postboost)



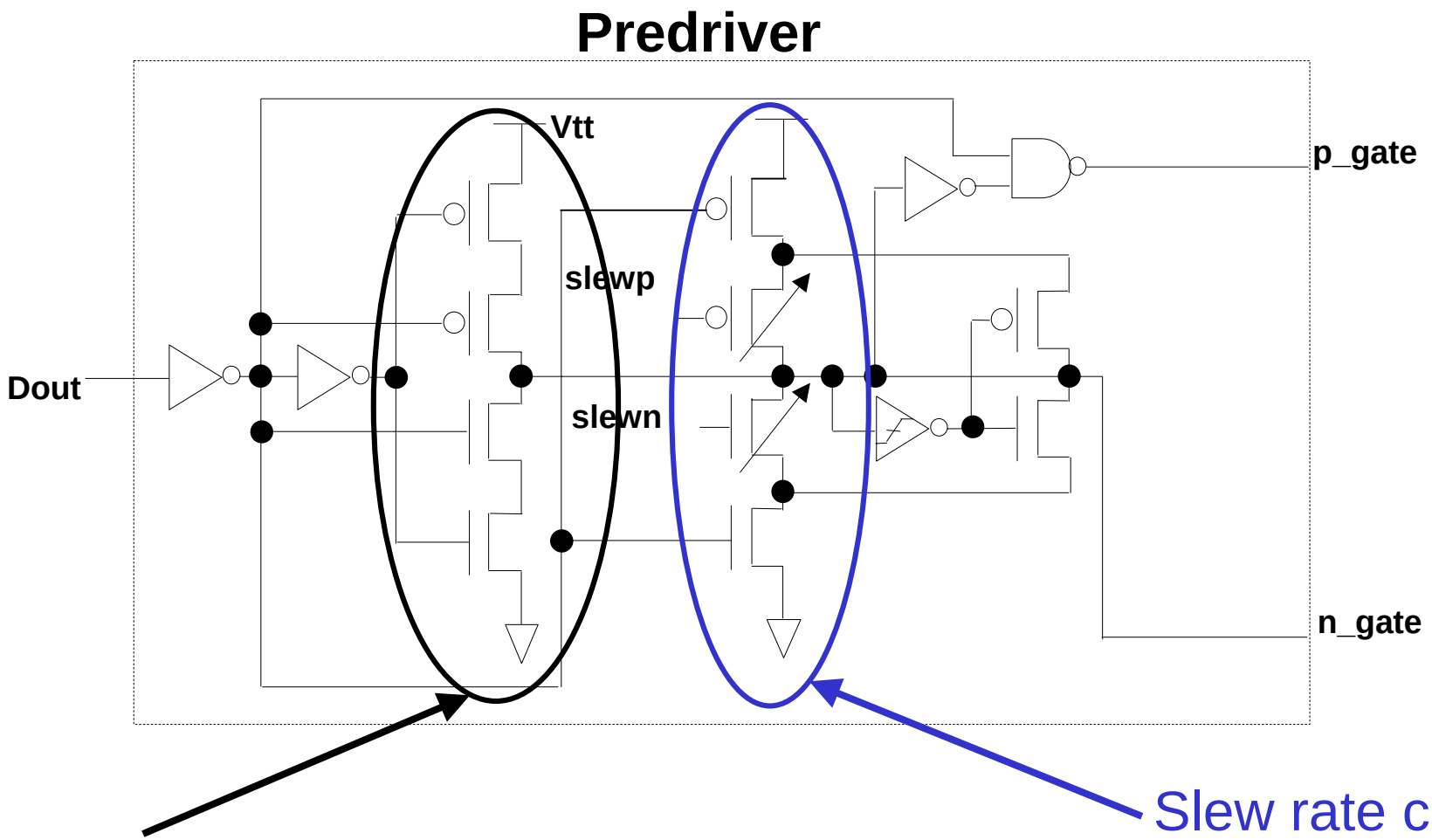


Pre/postboost Circuit

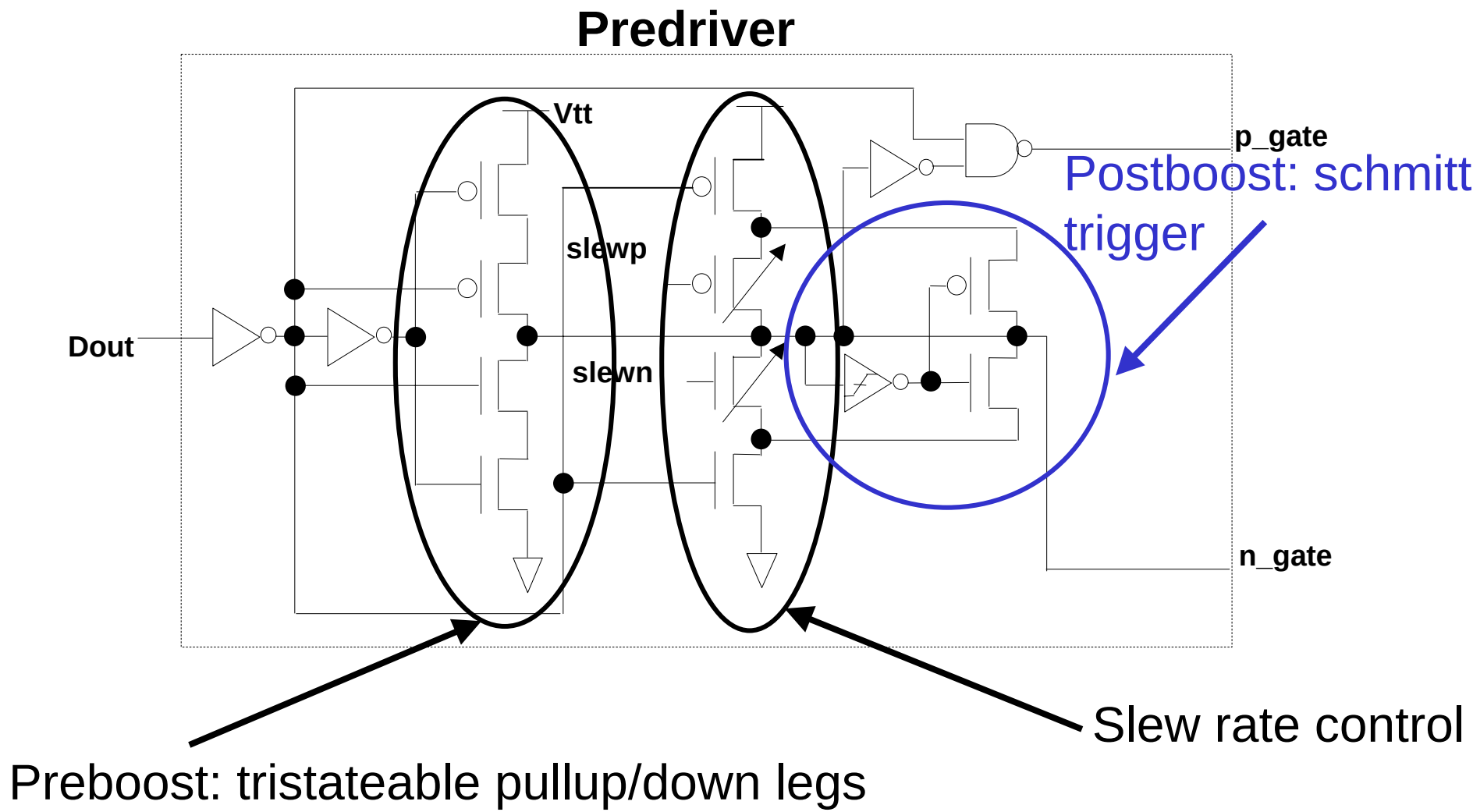


Preboost: tristateable pullup/down legs

Pre/postboost Circuit

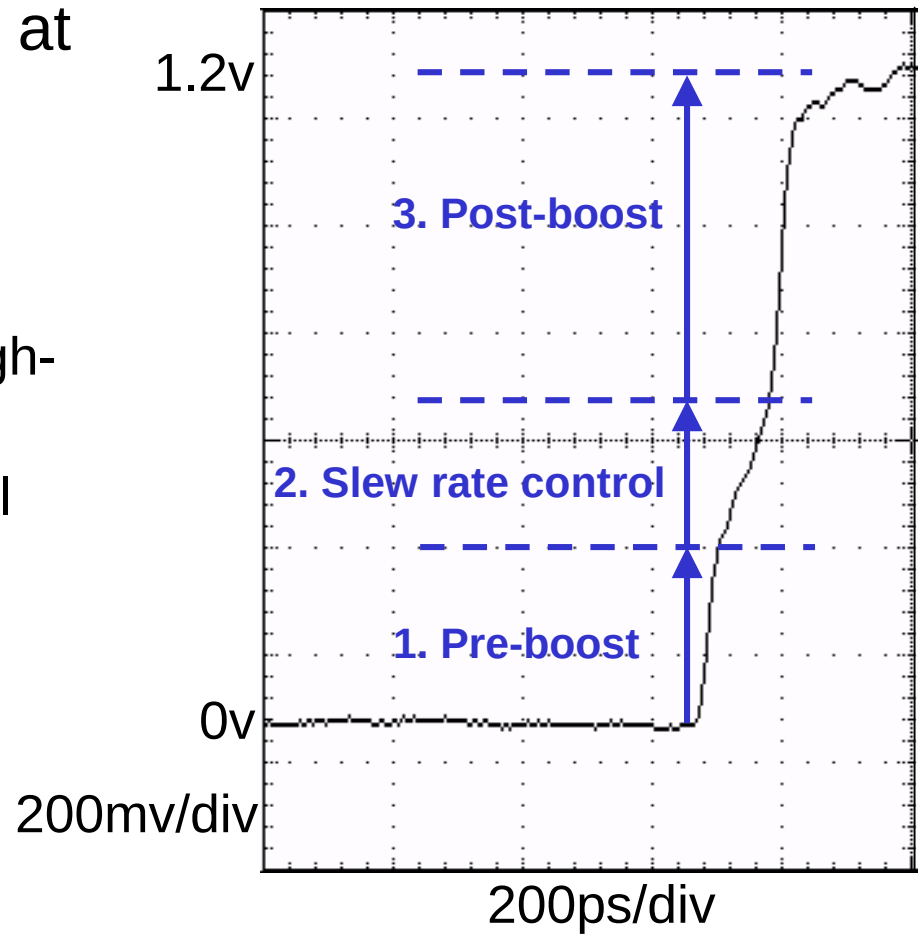


Pre/postboost Circuit



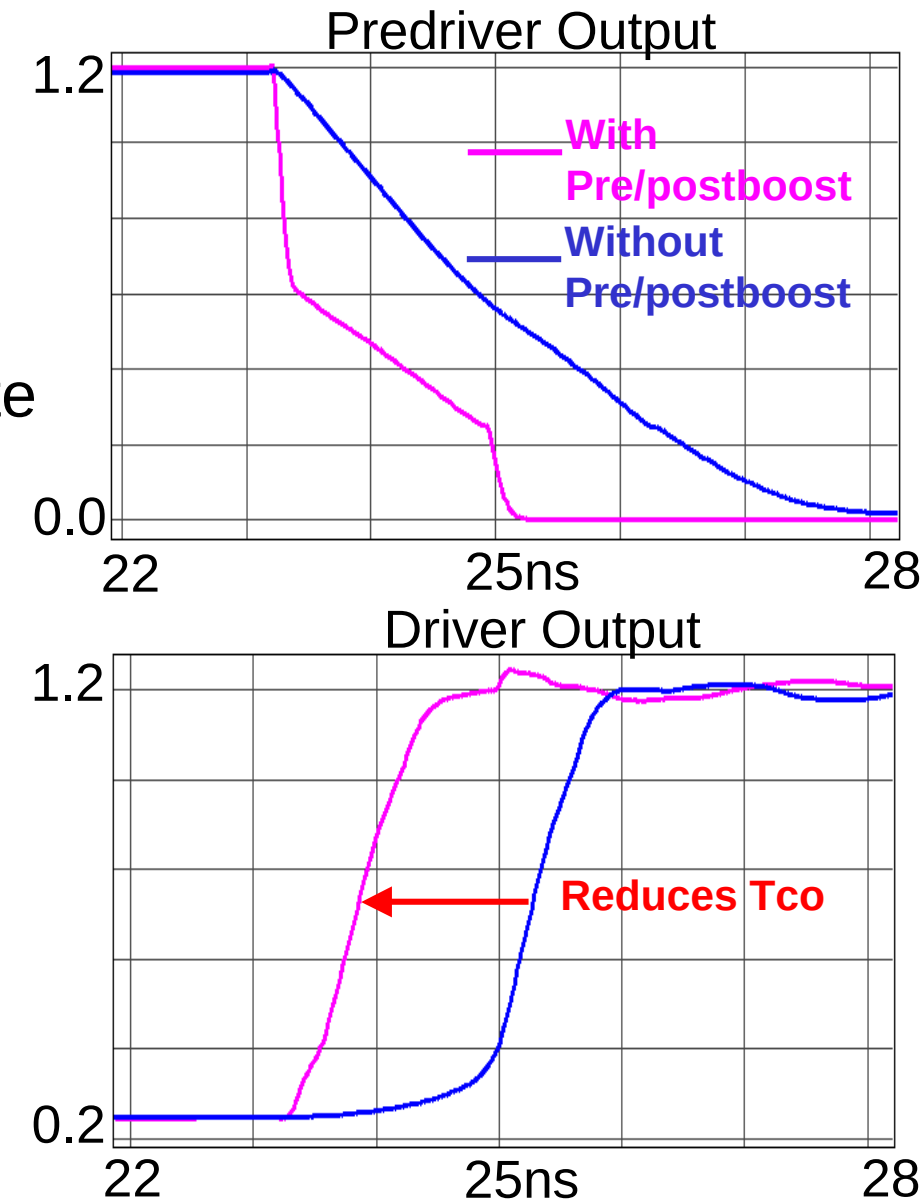
Pre/Postboost Waveform

- Pico-probed waveform at predriver output
- For rising edge output
  - Preboosted to ~Vt
  - Slew-rate control in high-gain region
  - Post-boosted to full-rail
- Opposite behavior for falling edge



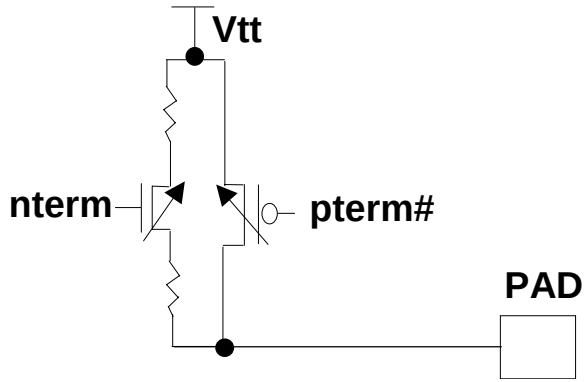
Purpose of Pre/postboost

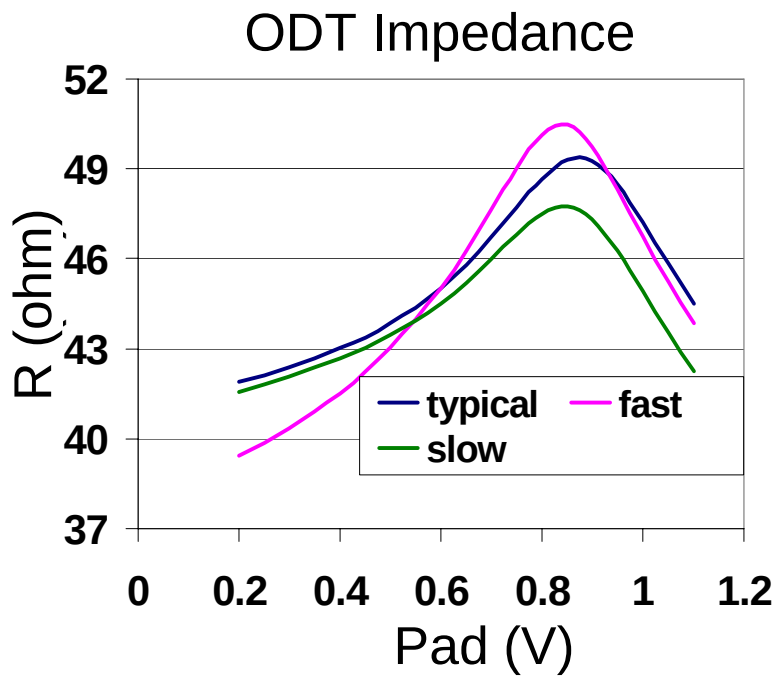
- Tco reduction
  - Enabling high speed operation
- Tightly-controlled edge rate
  - 1V/ns +/- 10%
- Linear edge rate near Vol and Voh



On-die Terminator

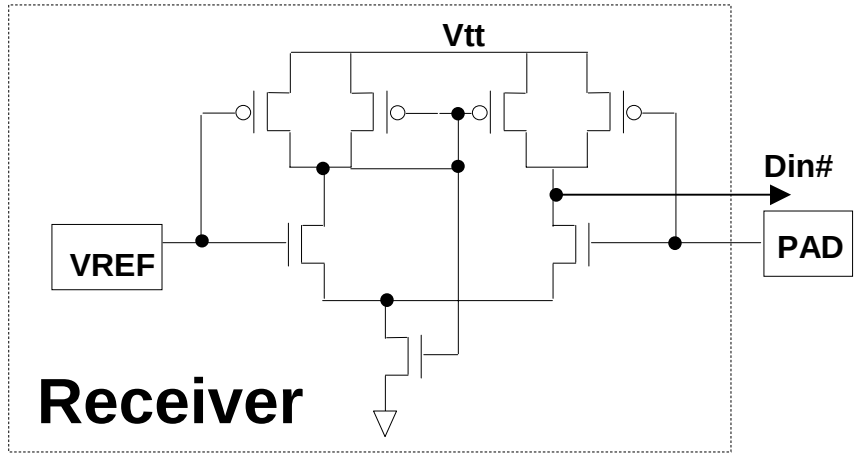
- Enabled on the end CPUs
- ODT implemented with parallel pmos and nmos devices
  - To obtain linear Zo characteristics @ 750mV
- Nwell resistors provide ESD protection & linearize Zo
- ODT is Process,Voltage & Temperature (PVT) compensated with Zo range 45ohm +/- 15%

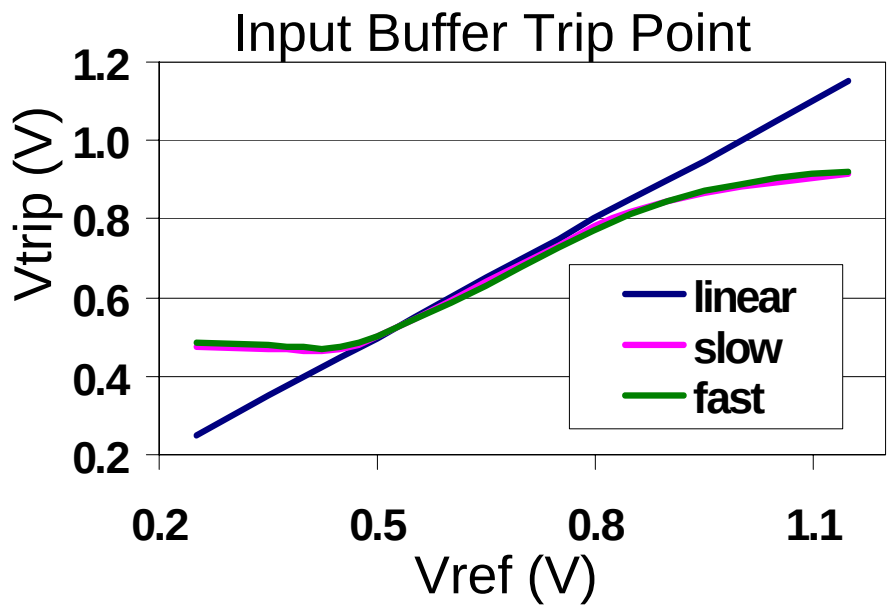




Input Buffer Characteristics

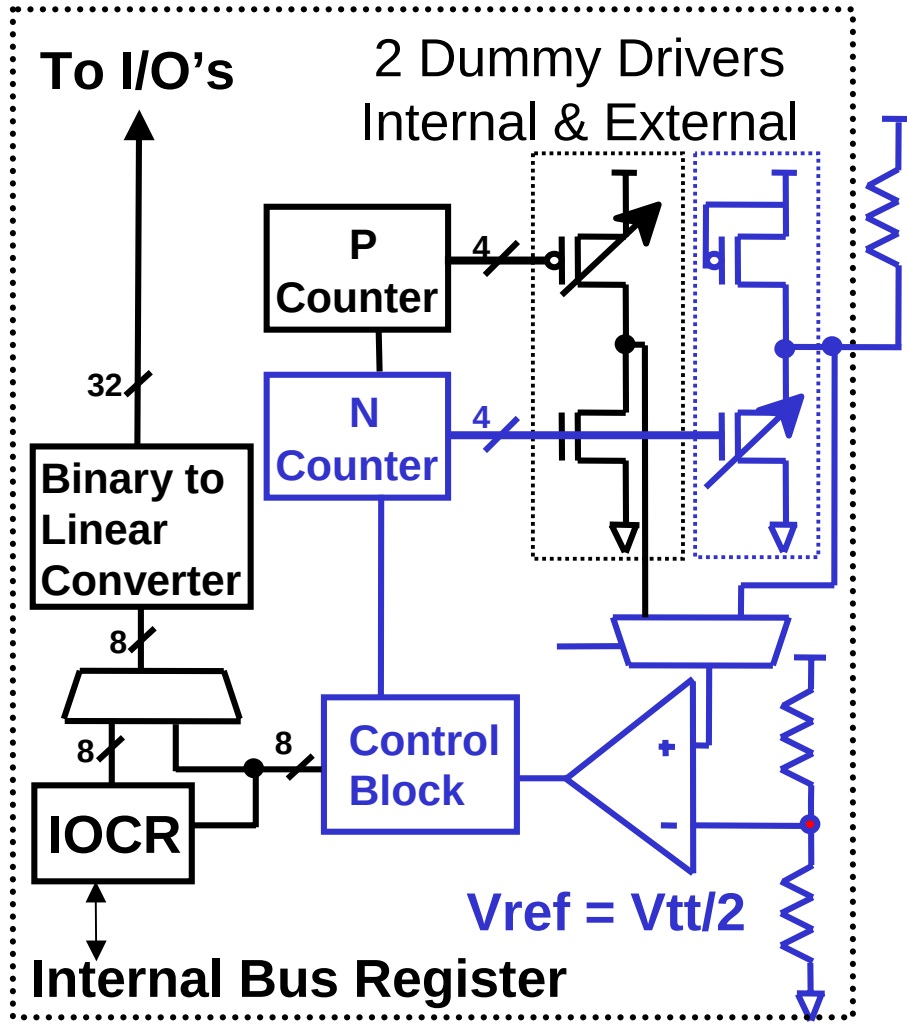
- Reference voltage generated on-die per buffer
- Vref centered at 750mV
  - Range of 600-900mV, 20mV increments
- Same diffamp for data & strobe
- Self-biased & unique differential gain property
- Trip-point “roll-off” provides noise immunity





PVT Compensation Technique

- Slew rate & ODT PVT
- Digital calibration scheme
  - External calibration



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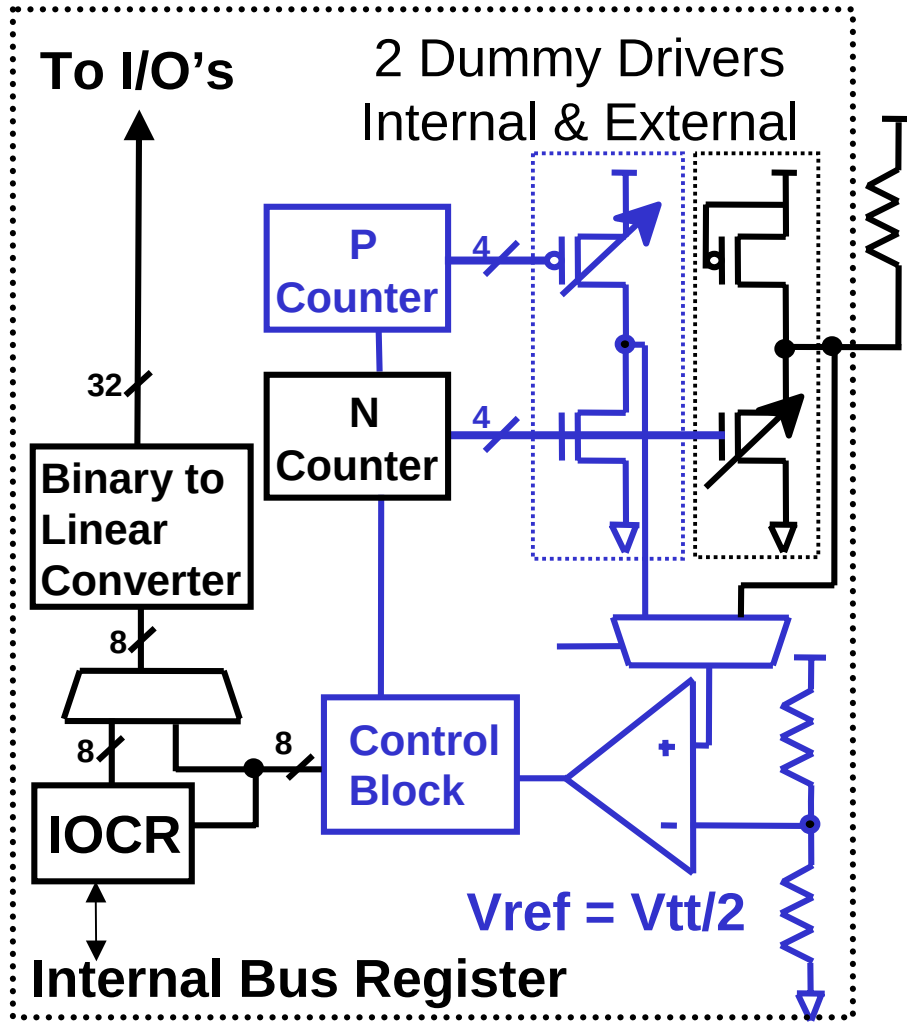
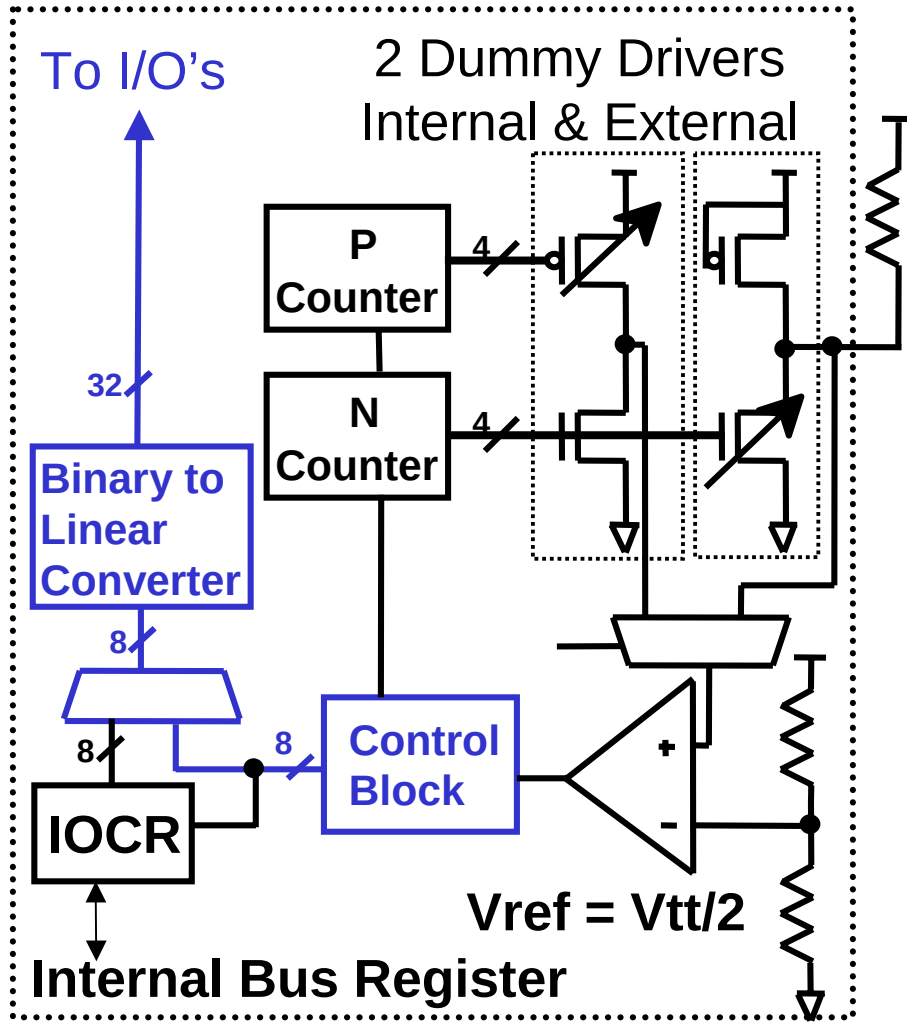


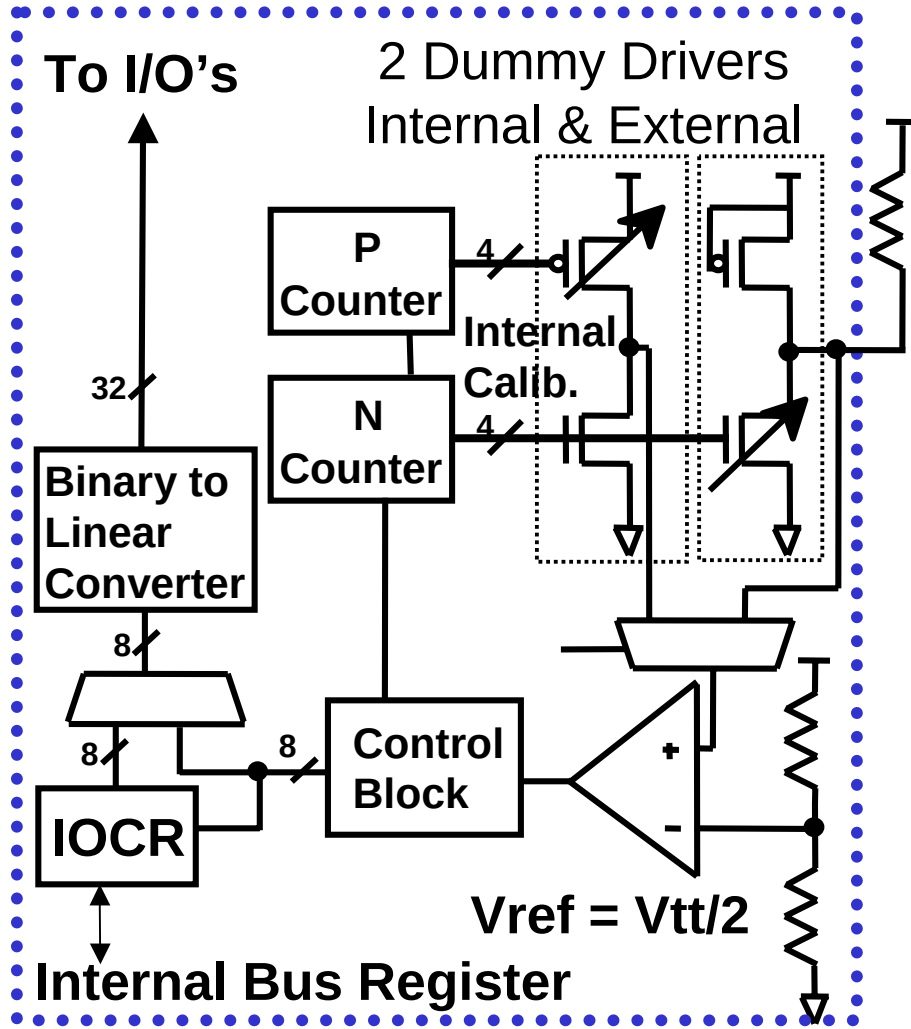
PVT Compensation Technique

- Slew rate & ODT PVT
- Digital calibration scheme
  - External calibration
  - Internal calibration
- One-time & continuous update
- Linear setting to avoid race

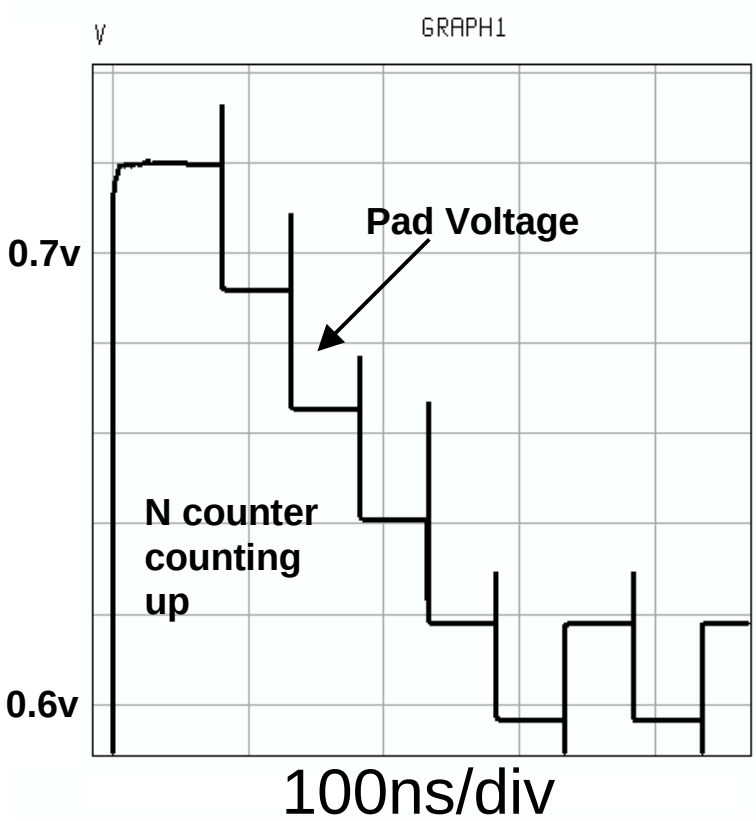


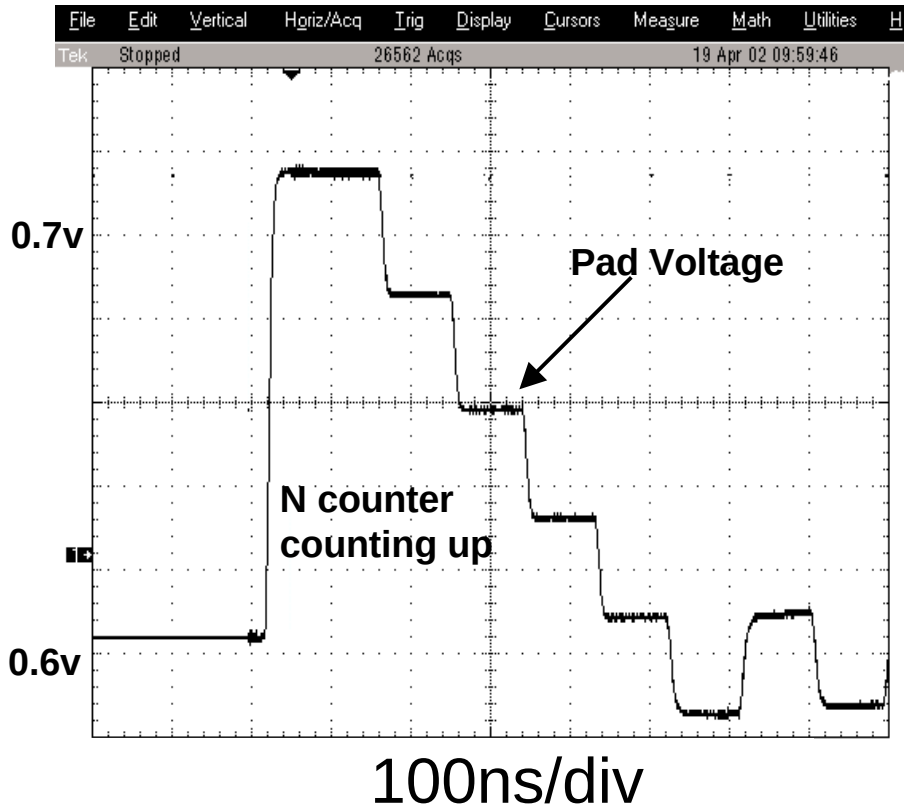
PVT Compensation Technique

- Slew rate & ODT PVT
- Digital calibration scheme
  - External calibration
  - Internal calibration
- One-time & continuous update
- Linear setting to avoid race
- Powered by Vtt to guarantee functionality in case of Vcc failure



PVT Results



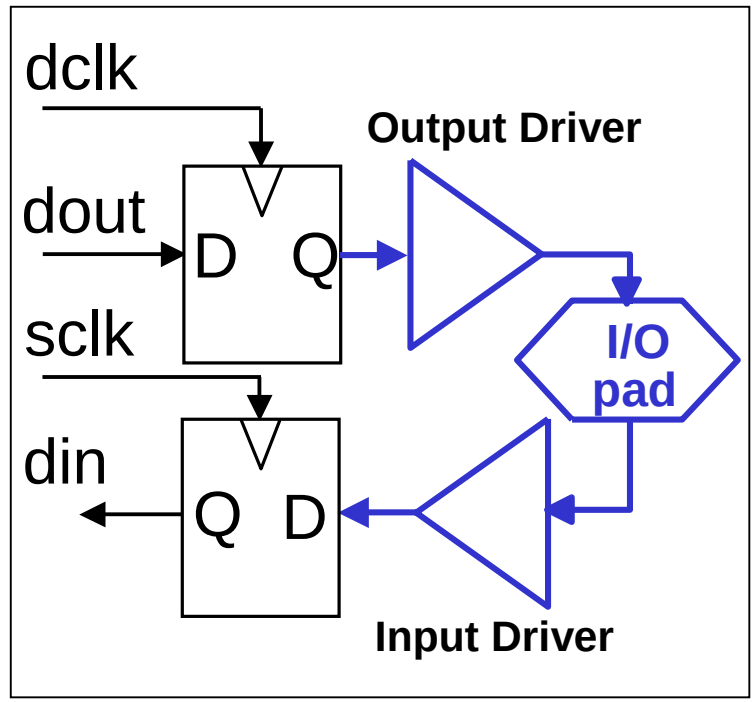


Simulation waveforms

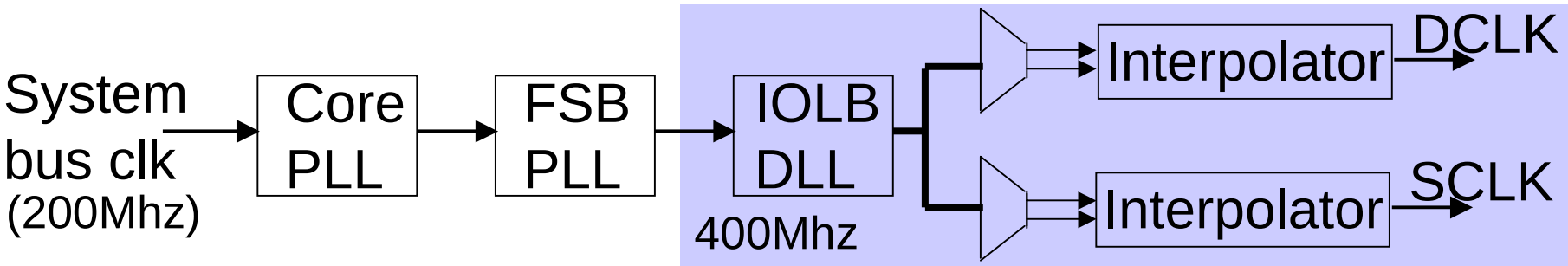
Oscilloscope waveforms

I/O Loopback (IOLB) Operation

- Loop time is tested by shifting sclk closer to dclk
- Loop stressed per pin
- Sticky latch (pass or fail)
- Per pin 4-bit pattern generator
- Rising & falling edges tested individually

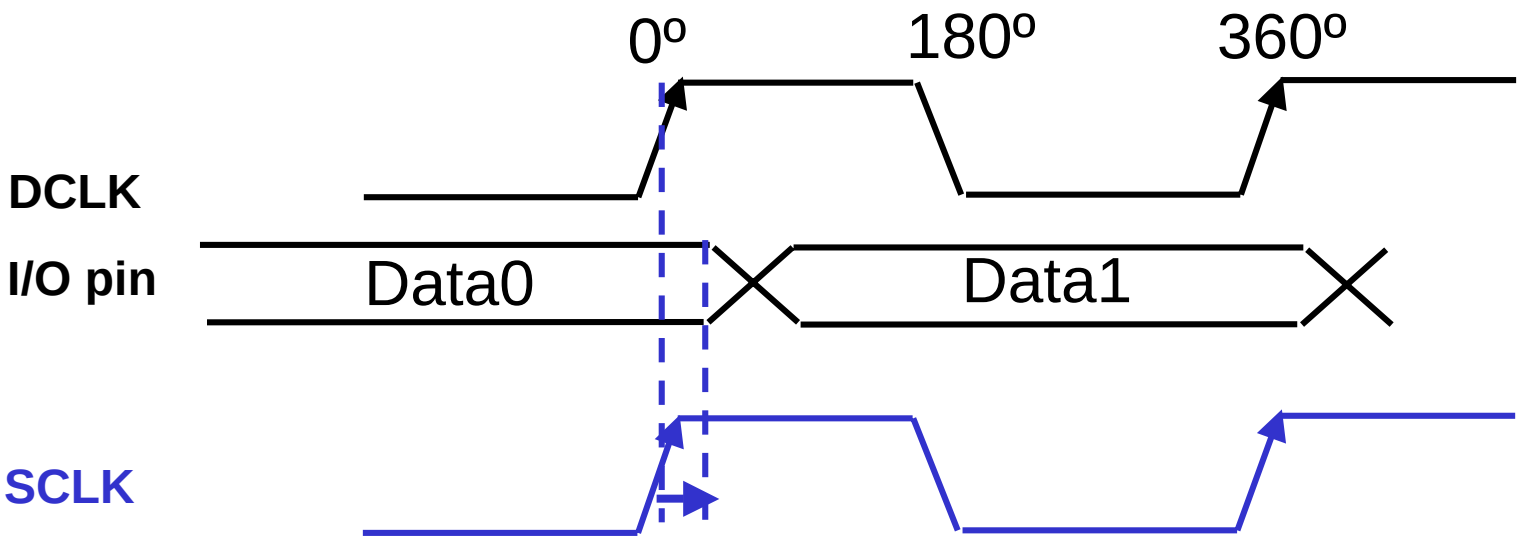


IOLB Clocking



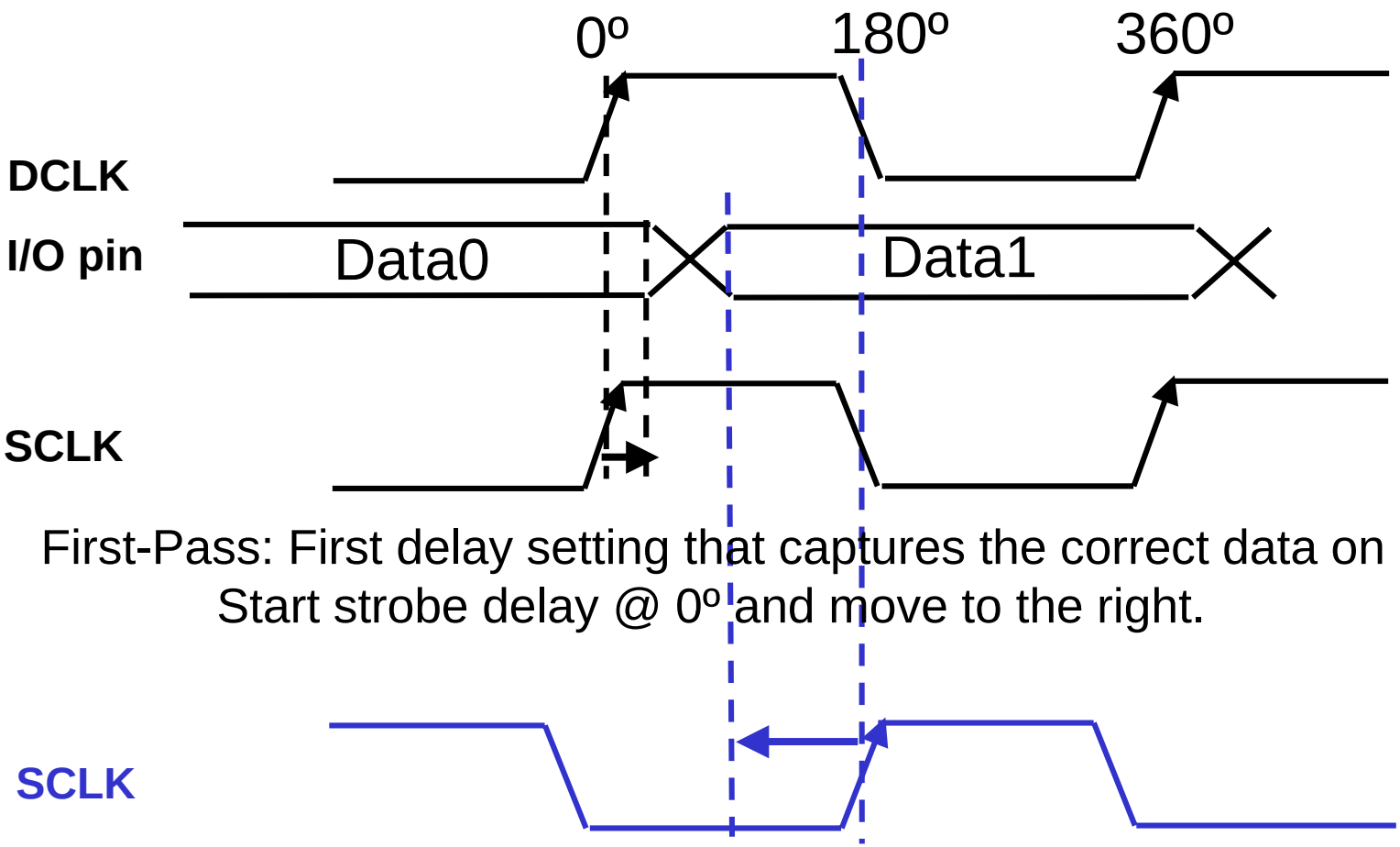
- DLL generates two dedicated test clocks.
  - DCLK timing is fixed to 0deg
  - SCLK timing is programmable in T/(8*15)
    - 8 phases provided DLL
    - 15 refined phases generated by interpolator
    - 1 tick = ~21ps

First and All-Pass



First-Pass: First delay setting that captures the correct data on any cycle
Start strobe delay @ 0º and move to the right.

First and All-Pass



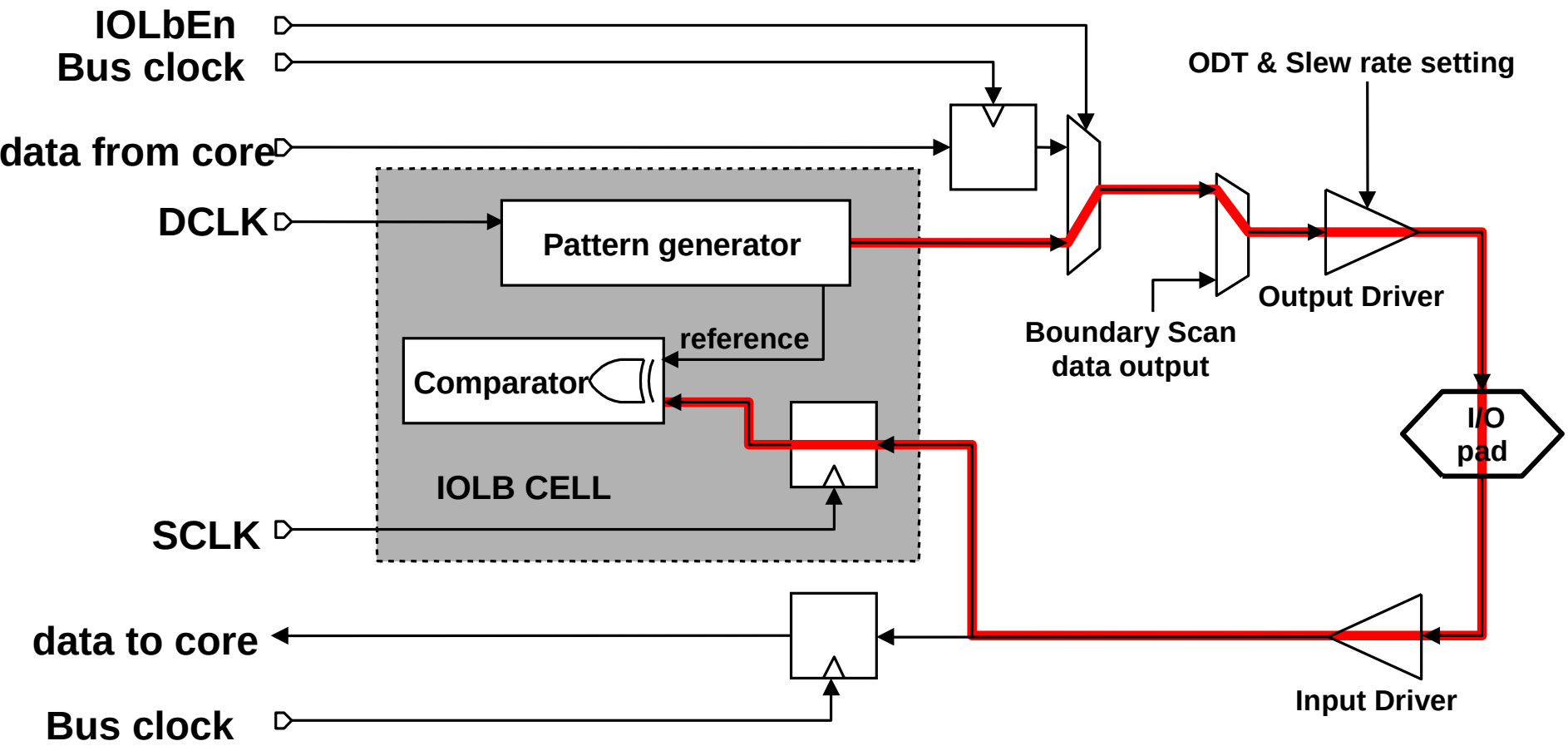
First-Pass: First delay setting that captures the correct data on any cycle

Start strobe delay @ 0º and move to the right.

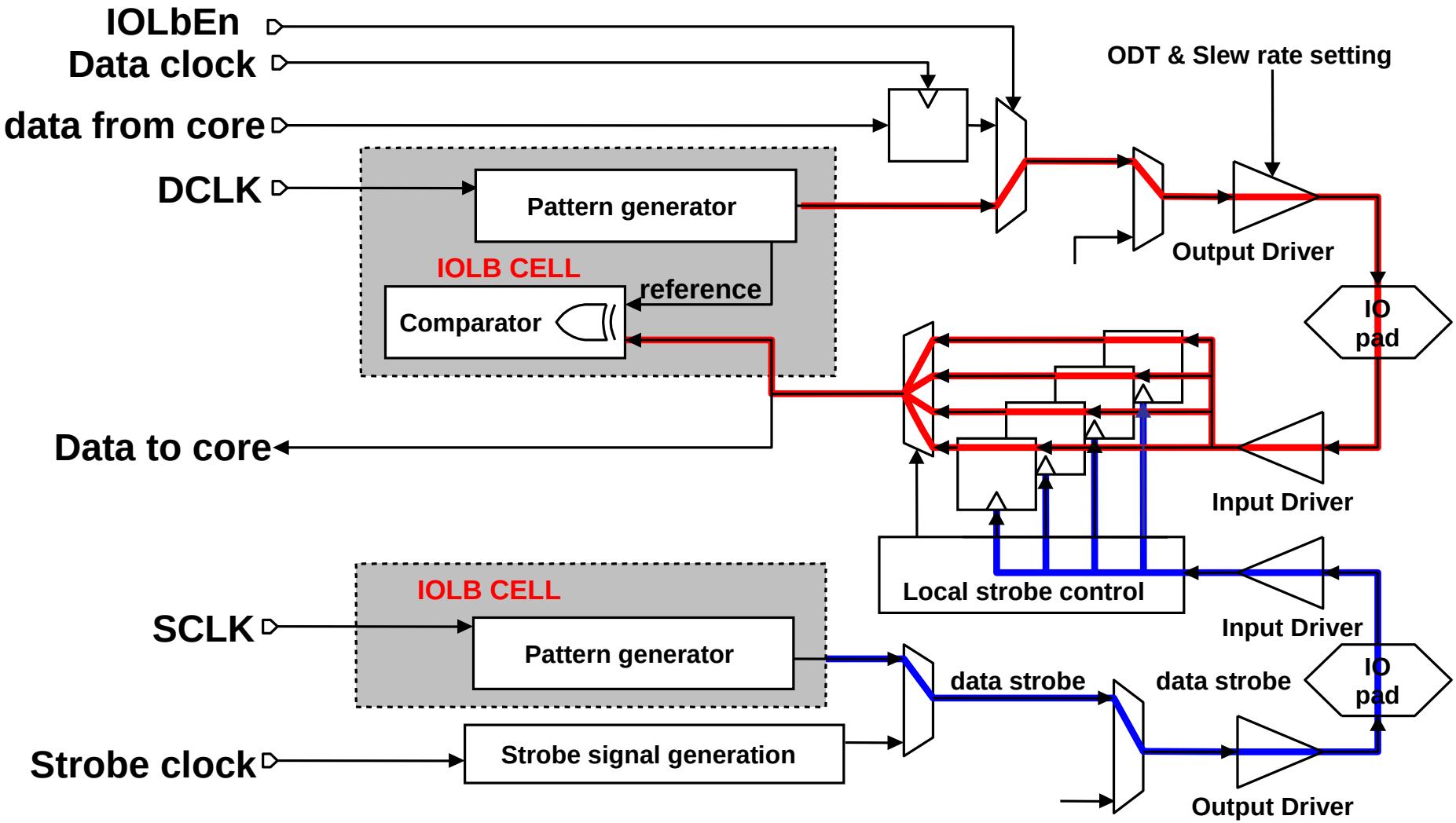
All-Pass: First loopback delay setting that captures the correct data on all cycles

Start strobe delay @ 180º and move to the left.

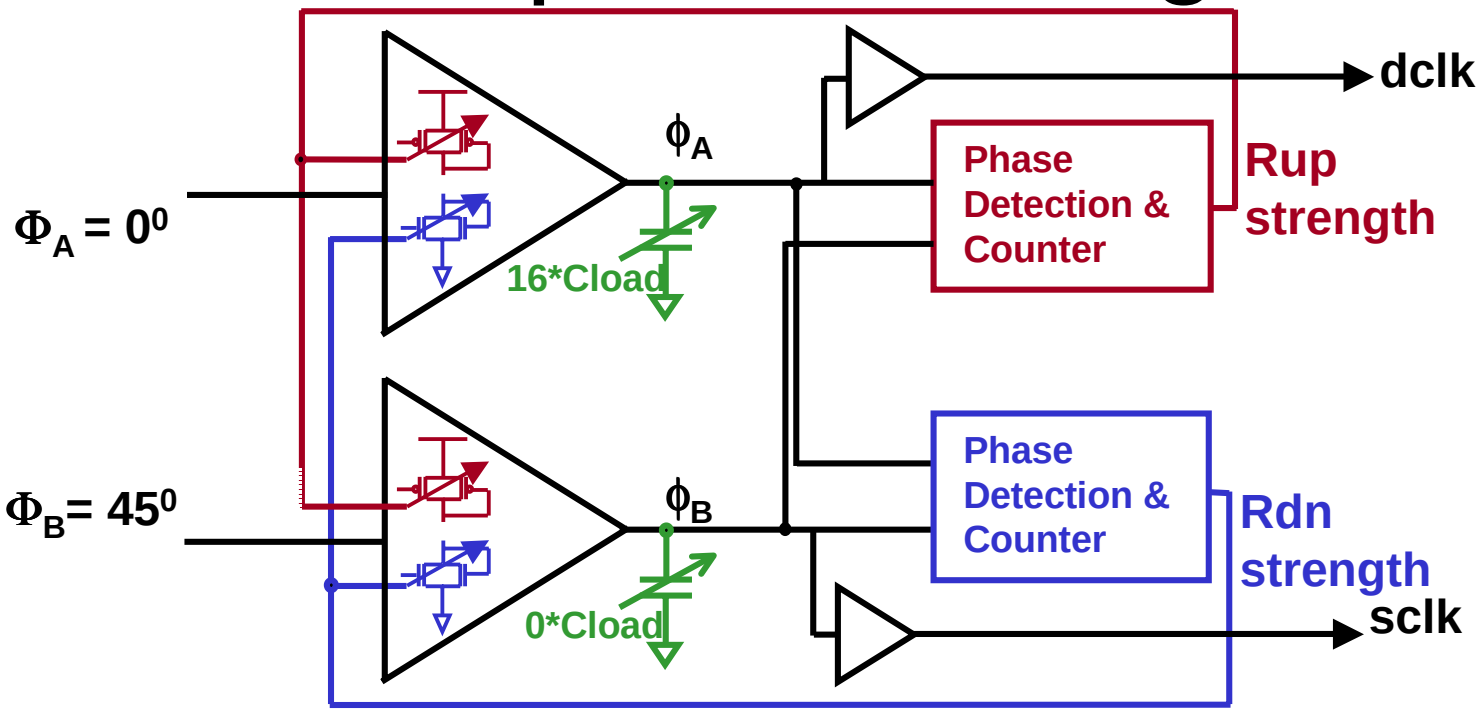
IOLB Common Clock Diagram



IOLB Source Synchronous Diagram

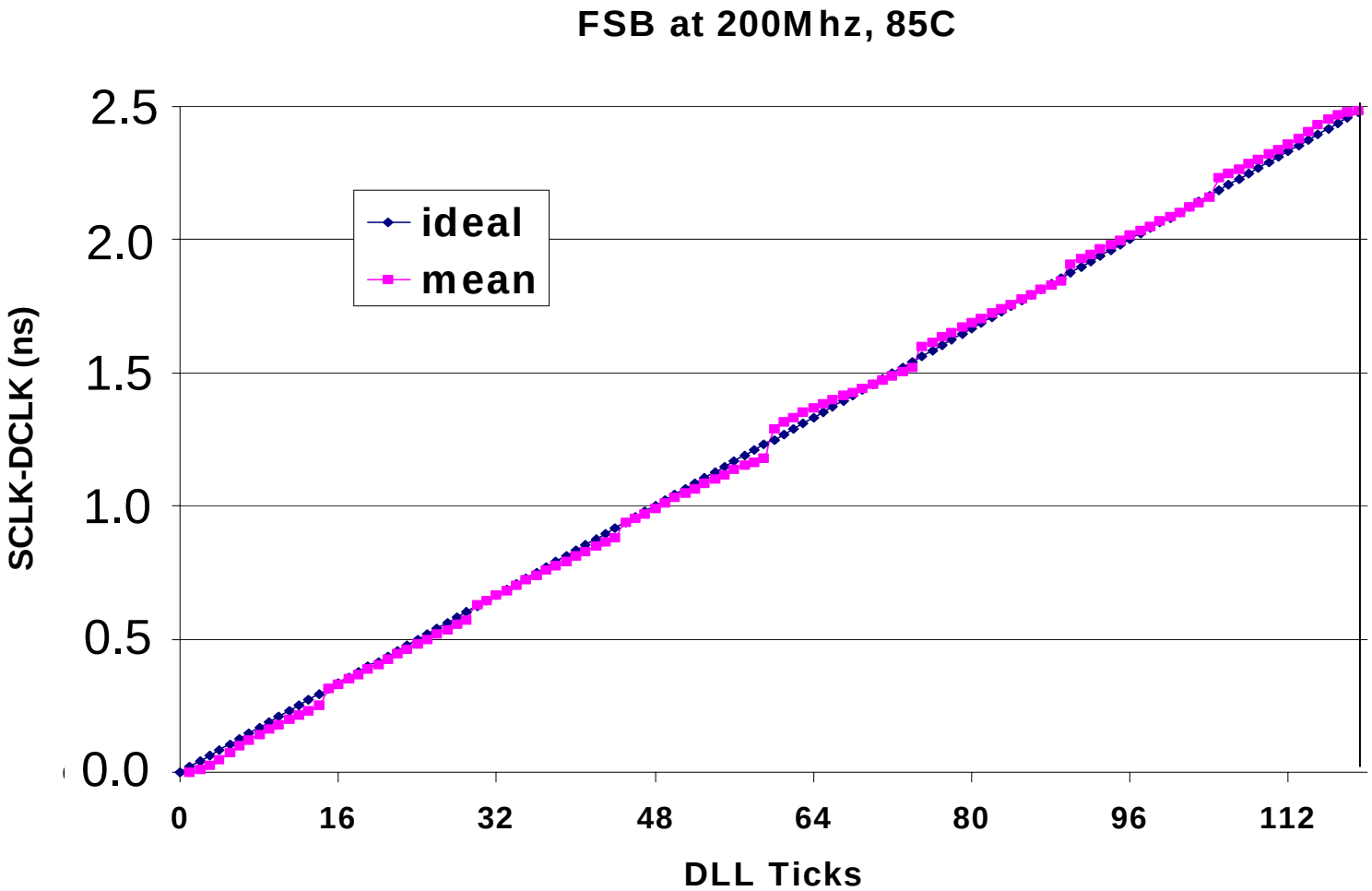


Interpolator Design



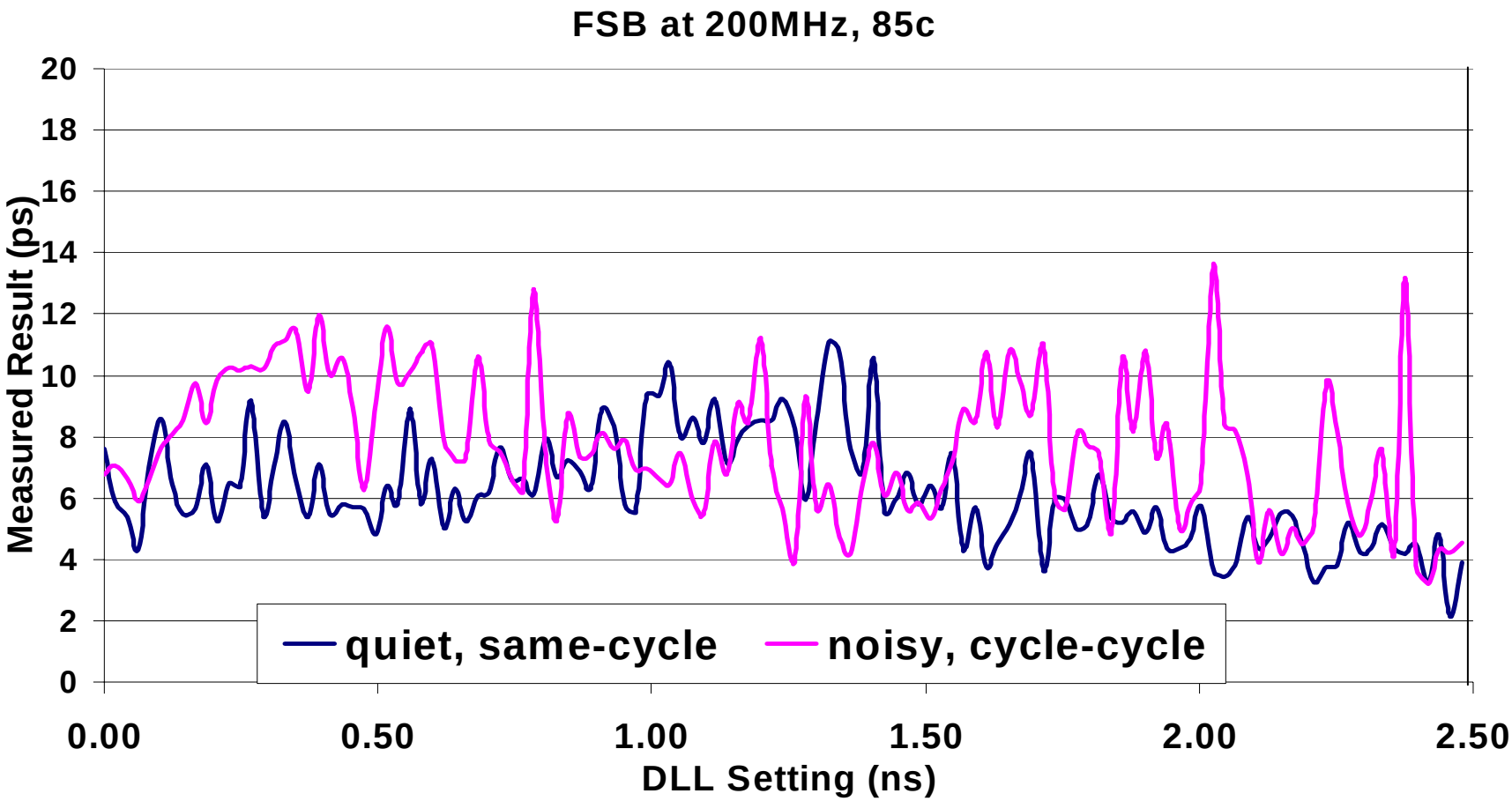
- RC-based interpolator
  - R value is determined during calibration
  - C value is used as interpolation steps (DLL phase/15=21ps)
- During calibration
  - Upper path is 0^0, 16*Cload; lower path is 45^0, 0*Cload
  - Modify R value until both paths have zero skew

DLL & Interpolator Linearity



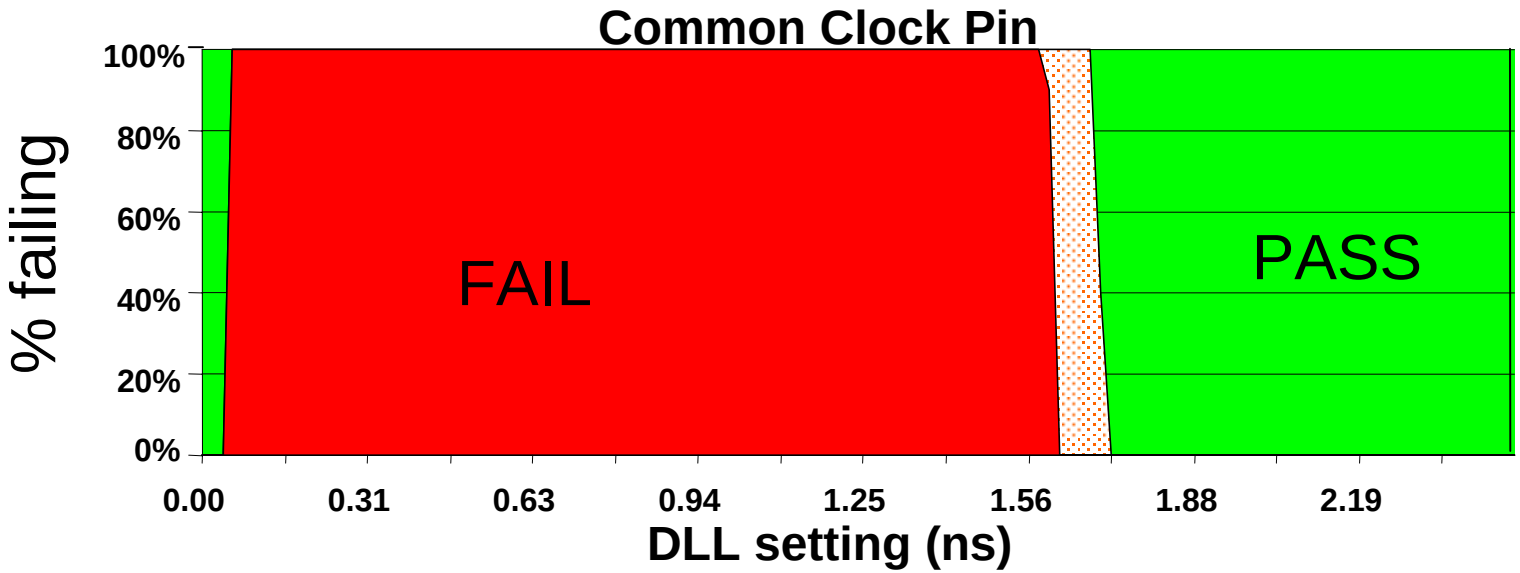
- DLL & interpolator is accurate within +/- 1 tick +/- jitter

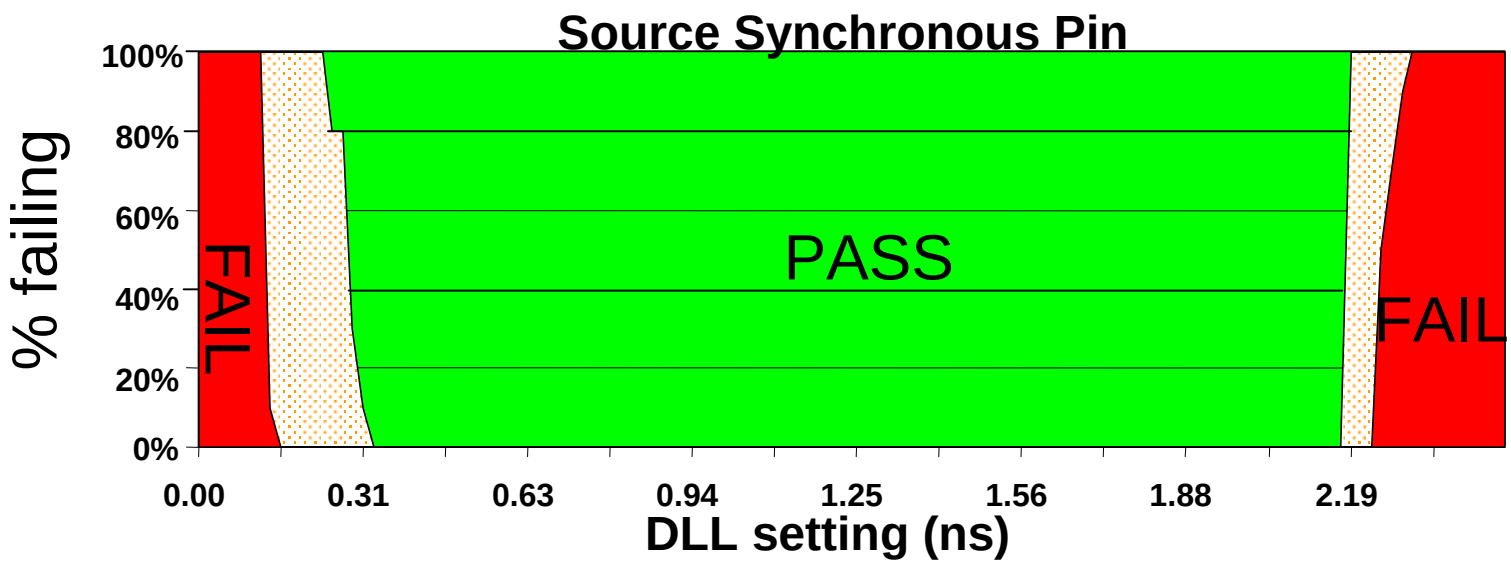
DLL & Interpolator Jitter



- DLL & interpolator jitter is less than 15ps max

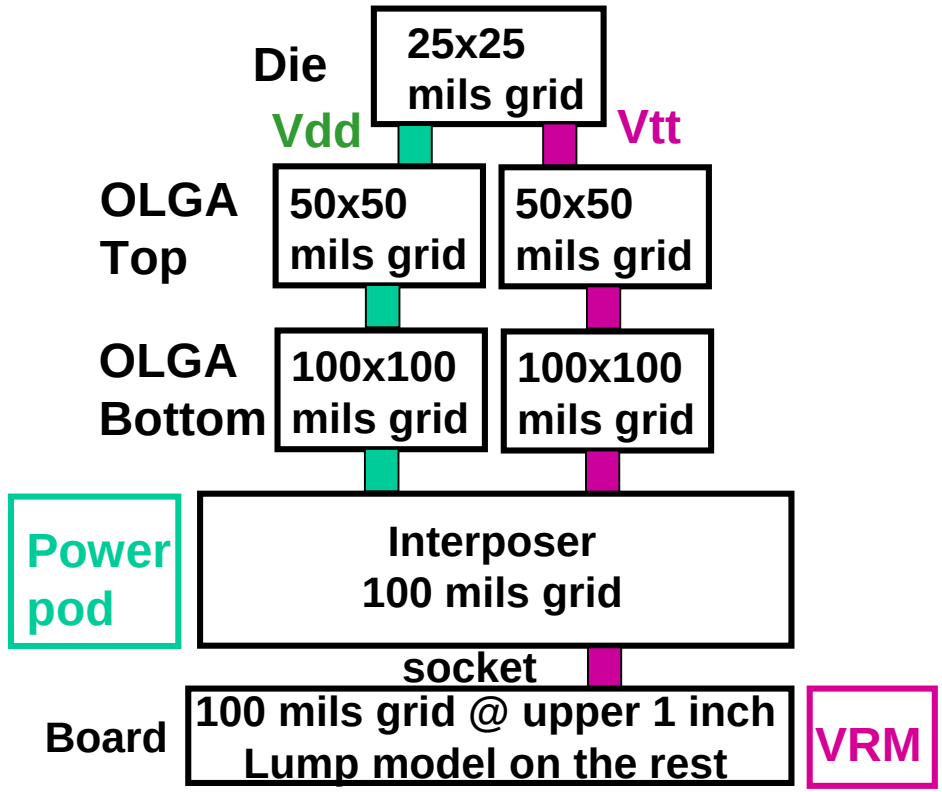
Search Results





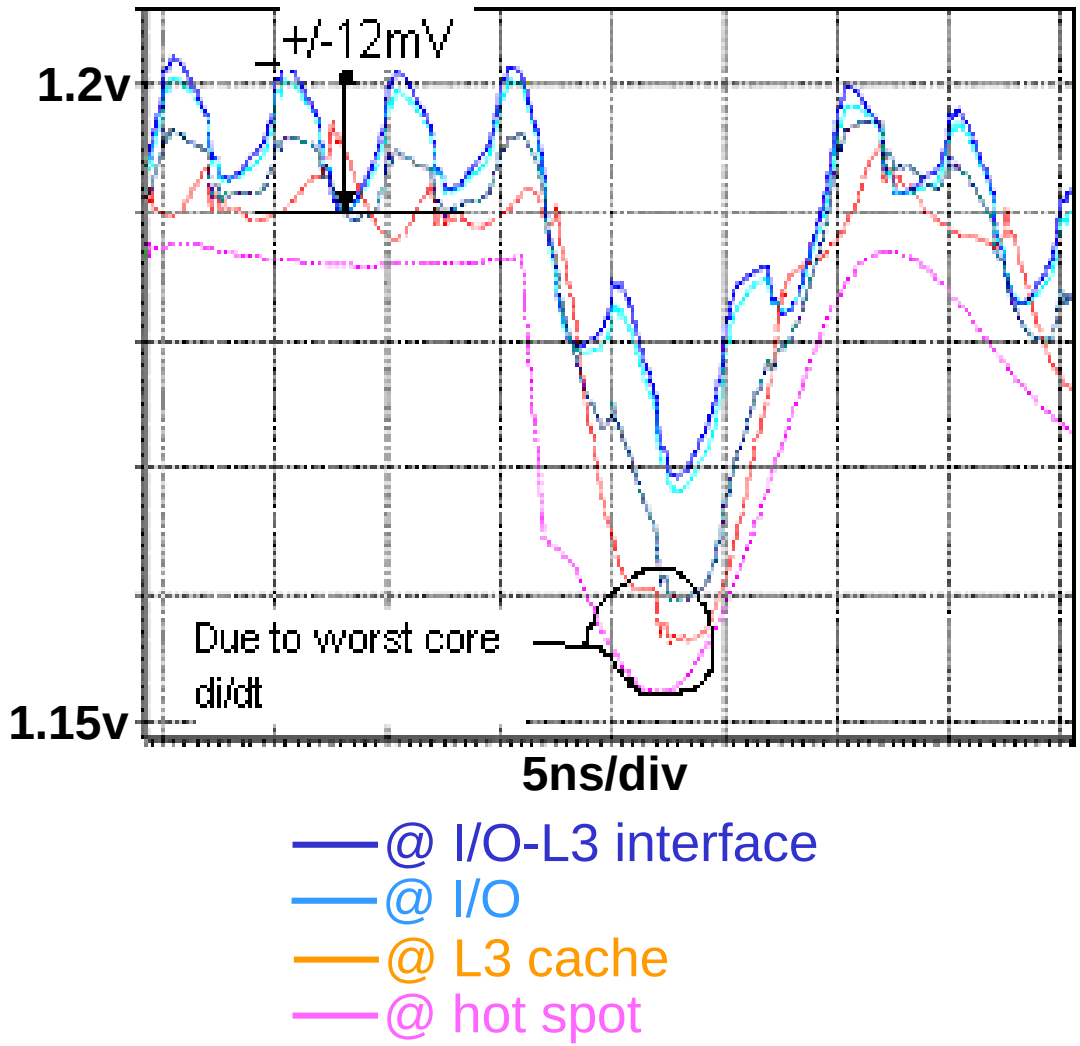
I/O Power Supply Modeling

- Integrated power delivery modeling
  - Distributed LRC models for Vdd and Vtt
  - Increasing grid area from die to motherboard



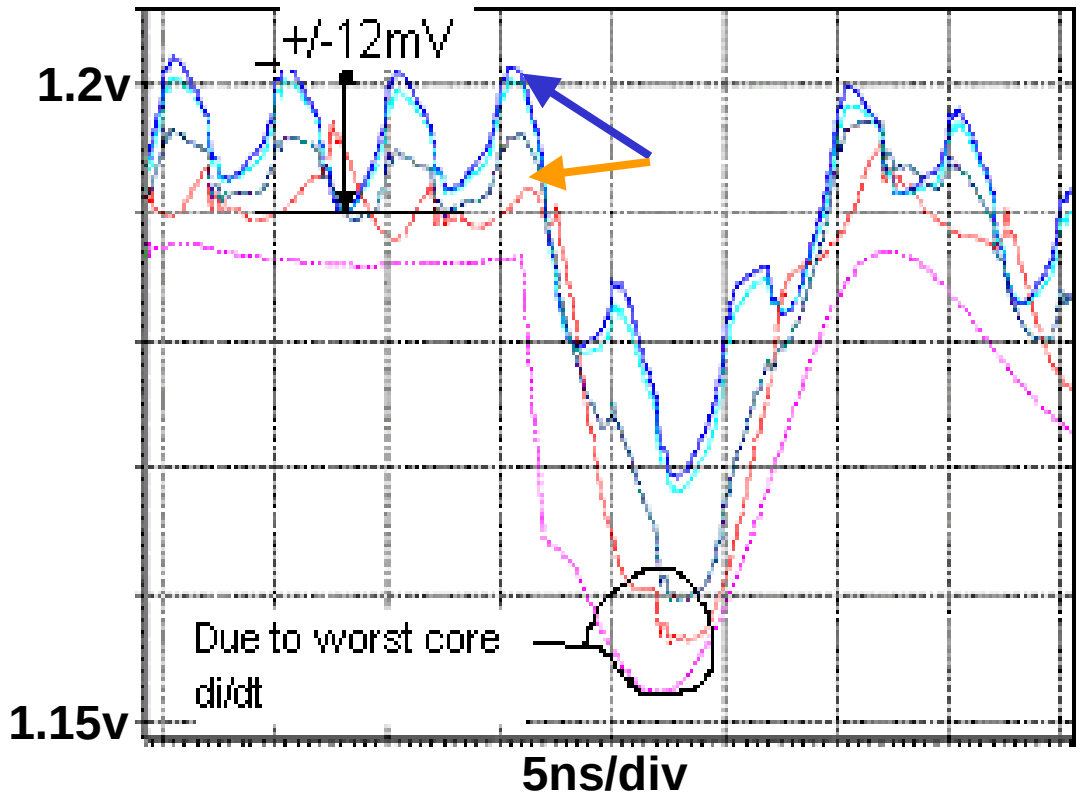
AC Noise

- Vtt noise is +/- 12mV



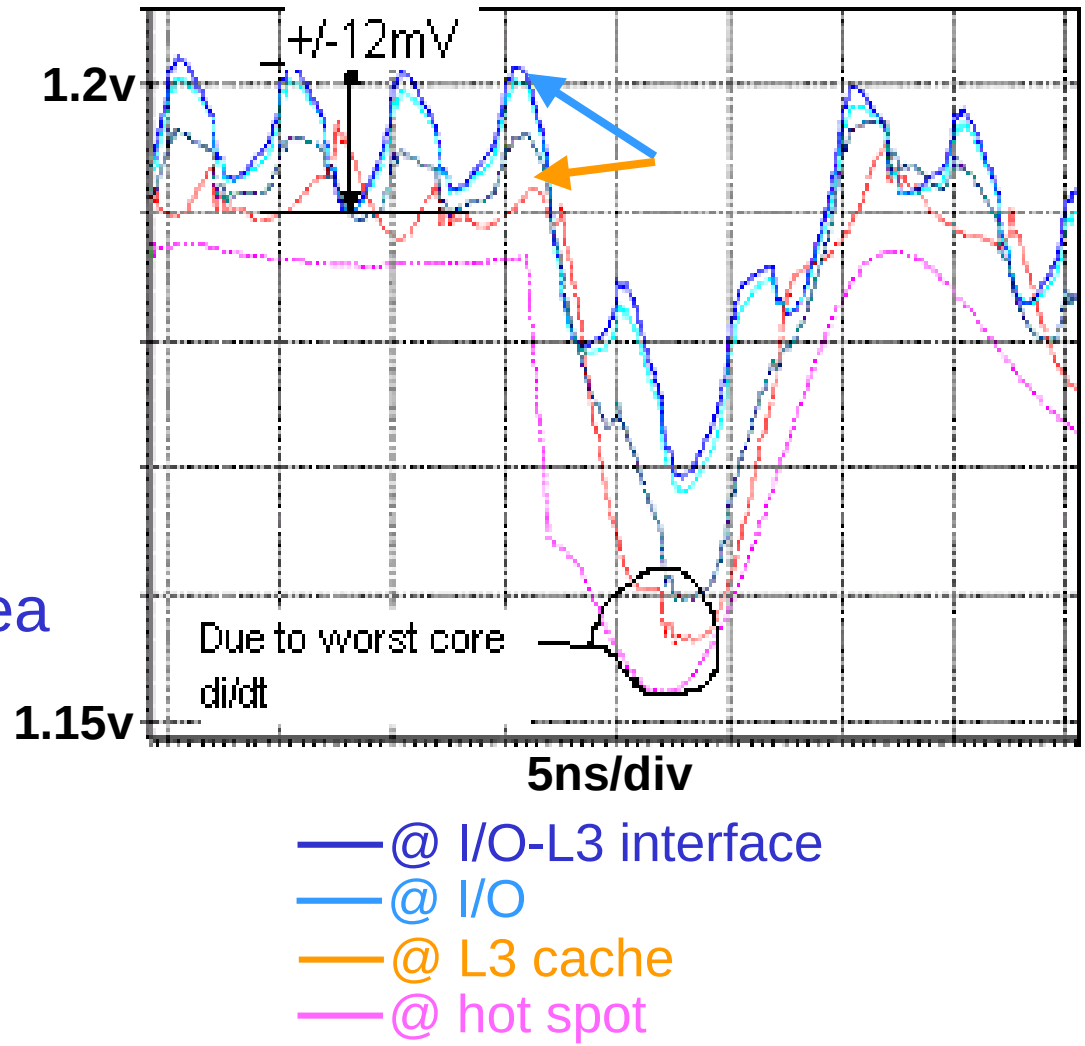
AC Noise

- Vtt noise is +/- 12mV
- Noise coupling
  - Vtt to Vdd by 9%

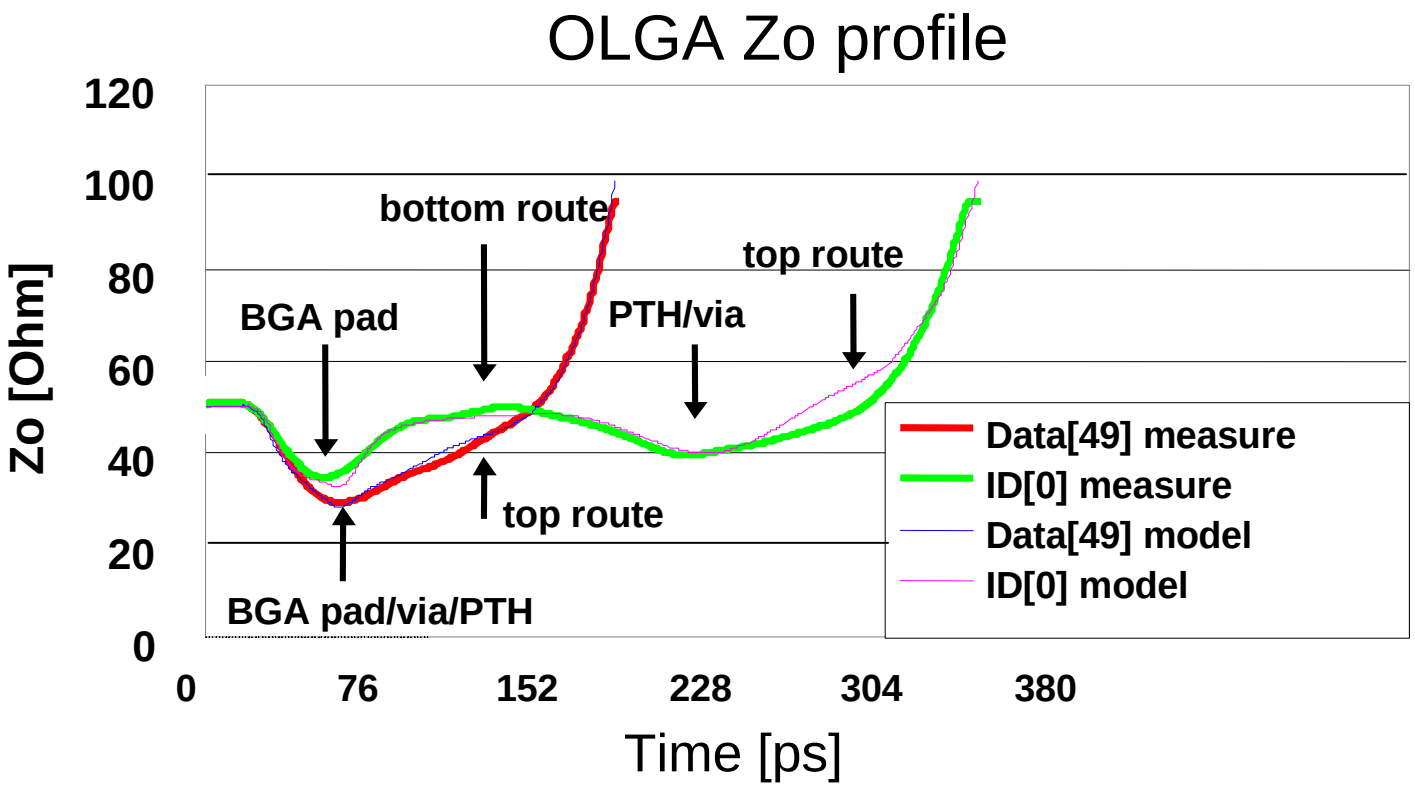


AC Noise

- Vtt noise is +/- 12mV
- Noise coupling
  - Vtt to Vdd by 9%
  - Vdd to Vtt by 1%
  - Neighboring cache is low power density area



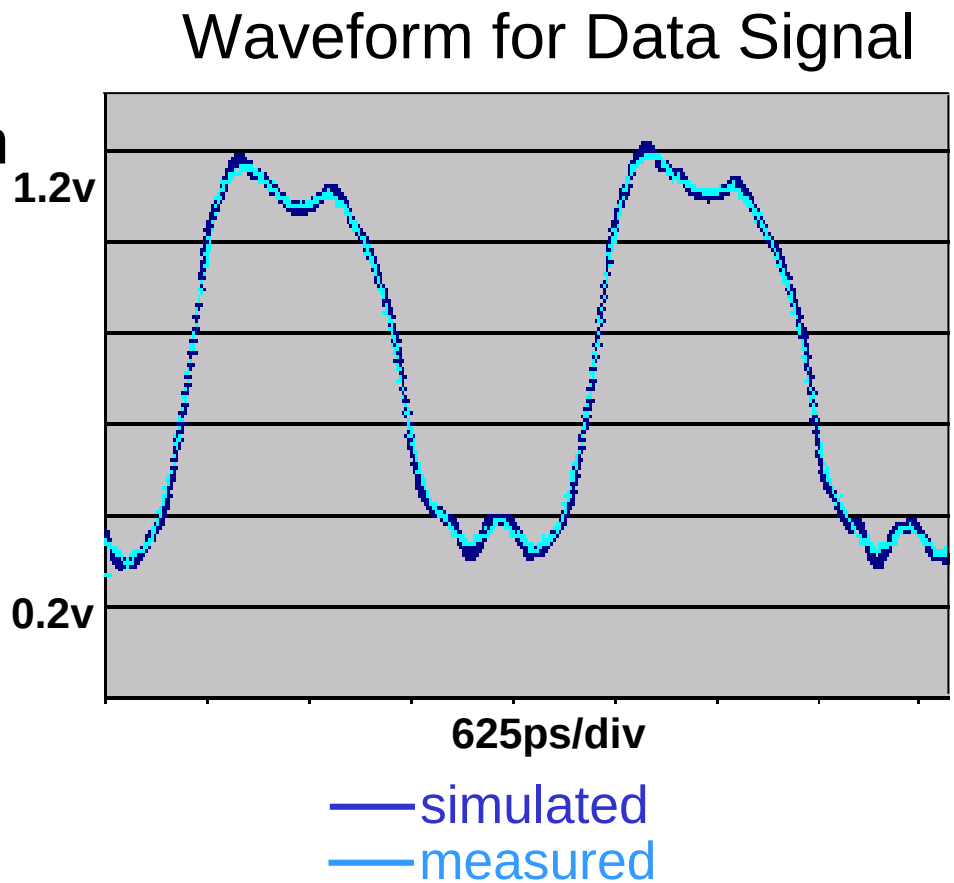
Pre and Post Si validation



- Package and board impedance is validated with TDR measurement before Si assembled.
- Measured at OLGA land toward C4 bump

Correlation w/ Measurement

- Correlated measured and simulated data bit at known PVT condition.
  - Slew bits overwritten for correlation purpose
- Excellent correlation within 5%



Summary

- The Itanium® 2 Processor is targeted for high end server, requiring high bandwidth FSB to access and process large sizes of data
- Advanced packaging technology enables low inductance power delivery and short flight time
- State-of-the-art circuit design supports PVT compensated slew rate and ODT
- IOLB enables accurate high speed testing
- Accurate system and power model are essential for silicon and package design optimization